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Performance Analysis of 6T, 8T and 10T SRAM Cell in 45nm Technology

M G Srinivasa, Bhavana M S

Abstract: ***The rise of portable battery-powered devices has emphasized the significance of low power IC design. Embedded SRAM units have become indispensable elements within contemporary SOCs due to their substantial footprint. In research circles, SRAM is highly regarded as a semiconductor memory type, highlighting its crucial role in the VLSI sector. In this paper, 6T, 8T and 10T SRAM cells design is estimated for power consumption and delay. This proposed work presents the schematic, simulation of analysis of 6T, 8T and 10T SRAM cells at 45 nm technology. The Cadence Virtuoso software is utilized for creating schematic diagrams and layouts, while the ASSURA library is employed for conducting design rule checks (DRC) and layout versus schematic (LVS) comparisons to verify the alignment between the layout and the schematic. In the process, a low VDD of 1 V is taken for the design. The results shows that 10T SRAM is efficient in terms of read and write delay and power consumptions.***

Keywords: ***SRAM, Cadence. Tool, ASSURA, DRC, LVS***

I. INTRODUCTION

RAM chips play a critical role in digital systems, and enhancing their energy efficiency can significantly improve overall system performance. SRAM cells, a common choice in RAM design, offer faster speeds and lower power usage compared to DRAM, making them preferred. With the growing demand for portable devices, minimizing power usage is a key concern in VLSI design. This has spurred interest in developing low-voltage nano-sized SRAMs. However, reducing their size has also increased MOSFET leakage current, leading to higher power consumption. Consequently, there is increased emphasis on designing high-performance SRAMs, crucial for handheld devices, high-performance equipment, and processors. Voltage scaling is essential for achieving energy-efficient operation in digital circuits, reducing dynamic energy usage.

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II. CIRCUIT DESIGN AND ANALYSIS

A. 6T SRAM Cell

An SRAM cell typically comprises six MOSFETs. Within an SRAM cell, each bit is stored using four transistors (P1, P2, N1 and N3) arranged in two cross-coupled inverters. Two additional access transistors (N2 and N4) regulate cell access during read and write operations. The activation of the word line WL governs the behavior of N2 and N4, determining whether the cell connects to the bit lines BL and BL` for data transfer during both reading and writing processes.

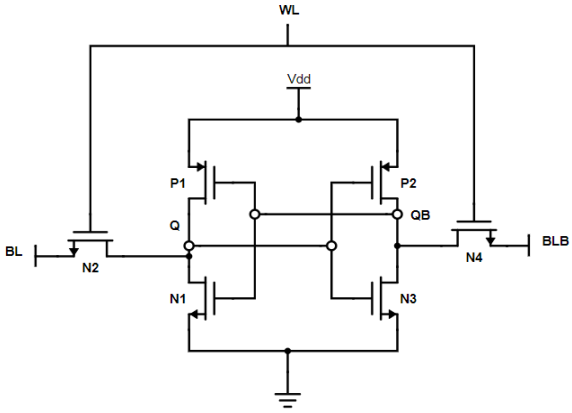

Fig.1: 6T SRAM Cell [6]

The SRAM cell has three states

1. Write
2. Read
3. Standby (Idle)

SRAM in read and write modes should exhibit "readability" and "write stability" separately.

The process of writing data starts with applying the intended value onto the bit lines. When writing a `0`, the bit lines are set to `0`, with BL` becoming `1` and BL becoming `0`, considering that the bit lines are initially charged to a high voltage. Conversely, to write a `1`, the states of BL and BL` are interchanged. After this, the word line (WL) is activated, facilitating the storage of the data into the cell [4].

During the reading process, the activation of the word line WL triggers the examination of the SRAM cell's state, accomplished through the involvement of a single access transistor (N4) and the bit line (BL). Owing to their extended length, bit line exhibits parasitic capacitance. The reading procedure commences by pre-charging both bit lines to VDD.

The extraction of output occurs from these bit lines throughout the reading operation. In contrast, when data is being written into the memory cell, the application of values onto the bit lines occurs simultaneously with the activation of the word line WL, which consequently activates both access transistors (N2 and N4) linked to the bit lines. This activation leads to a reduction in BL's voltage [4,6].

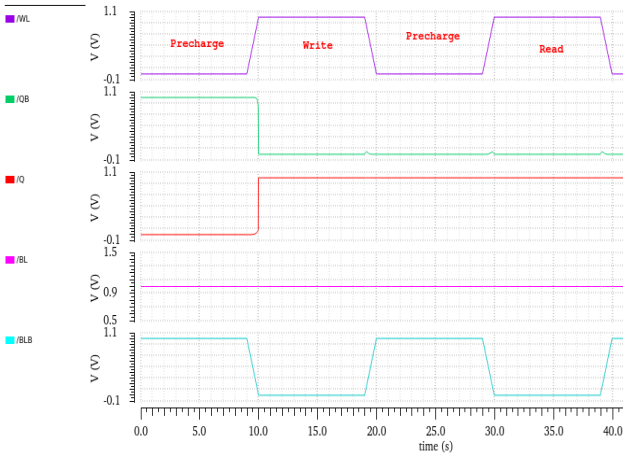

Fig 2: 6T SRAM Read and Write Operation

During the idle state, the word line is set to a low state, deactivating the access transistors. This action disconnects the inverters connected in a cross-coupled configuration from the bit lines via N2 and N4. As long as they remain connected to VDD. The two cross-coupled inverters formed by P1-N1 and P2-N3 will sustain each other, preserving the stored value in the SRAM.

B. 8T SRAM Cell

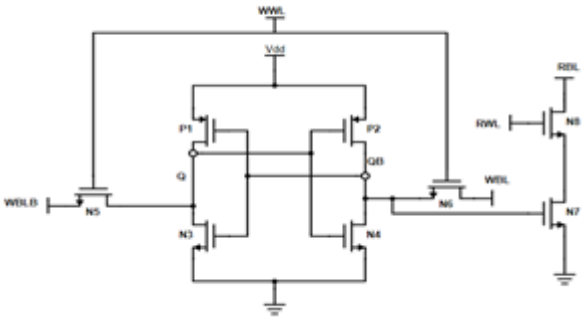

Fig 3: 8T SRAM Cell [7]

The 8T SRAM cell features distinct pathways for read and write operations, ensuring robust stability for both processes and serving as an effective design approach for SRAM cells. It comprises two-bit lines (WBL and WBLB) linked via NMOS access transistors N5 and N6 to the cross-coupled inverters. Additionally, the wire storing the bit connects to the gate of transistor N7, with its source linked to VSS [9][13][14].

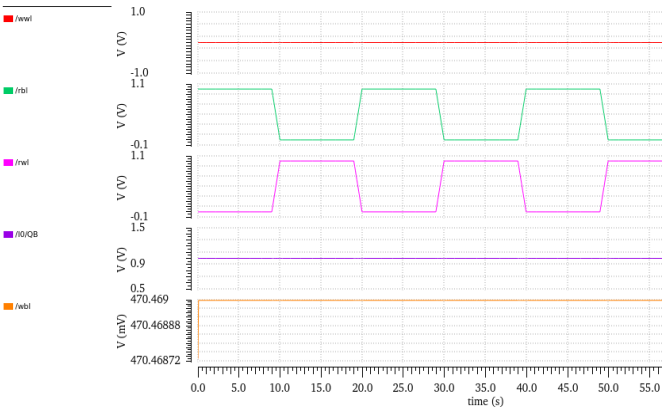

Fig 4: 8T SRAM Read Operation

The drain of transistor N7 is linked to the source of transistor N8, and the Read Word Line (RWL) controls the read operation by acting on the gate of N8. The Read Bit Line (RBL) is initially pre-charged to VDD and serves as the output during reading. When RWL is activated, transistor N5 turns on, and with the subsequent activation of N6 through RWL, the stored charge is drained, providing a complementary output for writing bit 1 through BL. This configuration utilizes pass transistors in the read pathway, with RWL controlling them through their connection to the gate of these pass transistors.

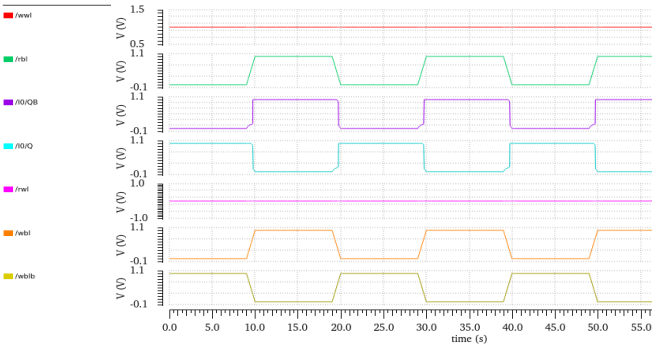

Fig 5: 8T SRAM write Operation

During write operation RWL is made low and complementary inputs are applied to WBL and WBLB. Outputs are observed in Q and QB nodes [2].

C. 10T SRAM Cell

The 10T SRAM consists of two cross coupled transistors P1, N3 and P2, N4 with two access transistors N5, N6. A separate read port of four transistors P3, N10, N8 and N9. The presence of extra transistors serves to interrupt the leakage current path from RBL when RWL is low, ensuring its independence from the current of data storage nodes [1][10][11][12]. The write access mechanism and fundamental data storage unit resemble that of a standard 6T SRAM cell. The power consumed is less than the 10T SRAM that uses differential pair [8]

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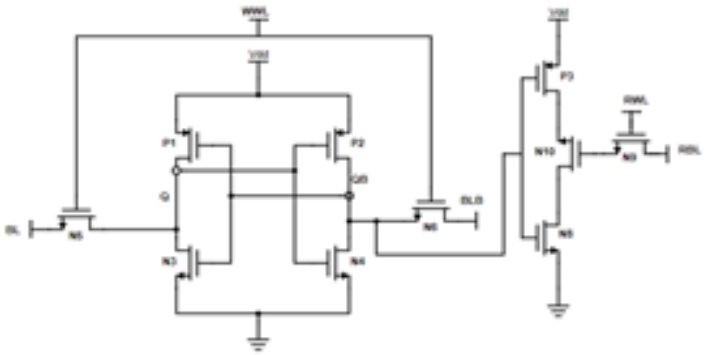

Fig 6: 10T SRAM Cell

Table.1: Power, Area, and Delay Analysis of SRAM Cells

SRAM	Read Power in µW	Write Power in µW	Read Delay in ms	Write Delay in ms	Power in W	Area in µm^2
6T	1.5589	69.533	350.755	313.385	75.149n	4.158
8T	10.548	23.15	285.126	81.72	1.0939µ	9.801
10T	18.803	18.24	255.453	57.94	38.217n	10.045

During a write operation, the word line (WWL) and bit line (BL/BLB) are activated based on the address of the cell to be written. RWL is made low. The data to be written is placed on the BL and its complement (BLB). The access transistors (N5 and N6) are turned on by the activated WWL, allowing the data on BL/BLB to be written into the storage nodes of the SRAM cell [5].

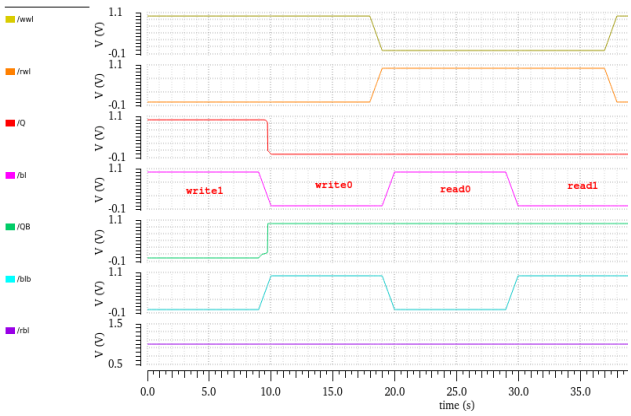

Fig 7: 10T SRAM Read and Write Operation

During a read operation, the word line (WWL) and RWL is made high. The access transistors connect the storage nodes to the bit lines (BL/BLB). The voltage levels on BL and BLB are sensed to determine the data stored in the SRAM cell. If BL is at a higher voltage level compared to BLB, it indicates a logic '1' stored in the cell and if BL is at a lower voltage level compared to BLB, it indicates a logic '0'.

III. RESULTS AND DISCUSSION

In conventional 6T SRAM Cell, N1 and P2 transistors have W/L ratio of 0.125 while all the other transistors have the ratio of 0.375. This is done to analyze the precharge, read and write stages clearly in the output. In 8T and 10T SRAM Cell, all the transistors have W/L ratio of 0.375. The supply voltage is 1V for the circuit.

The Table.1 (Column 2 and 3) and Fig. demonstrates the contrast between the power consumption for reading and writing of 6T, 8T and 10T SRAM Cells.

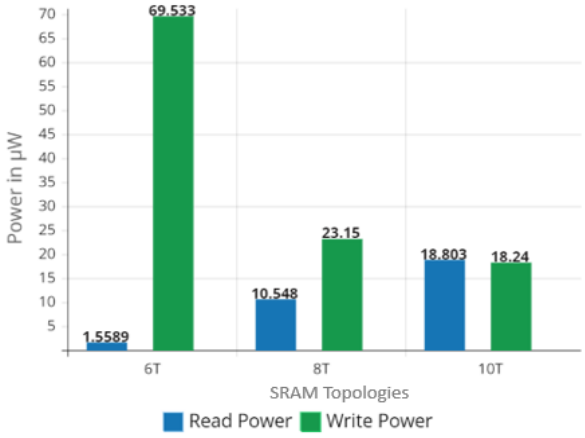

Fig 8: Comparison of Read and Write Power

Read power of 6T SRAM cell is 85.22% less than 8T. Read power of 6T SRAM cell is 91.7% less than 10T SRAM. Similarly, write power of 8T SRAM is 66.7% less than 6T SRAM. 10T SRAM has 73.76% of decreased write power than 6T SRAM. From this we observe that when read power increases at the same time write power decreases, with increase in transistor sizing [3].

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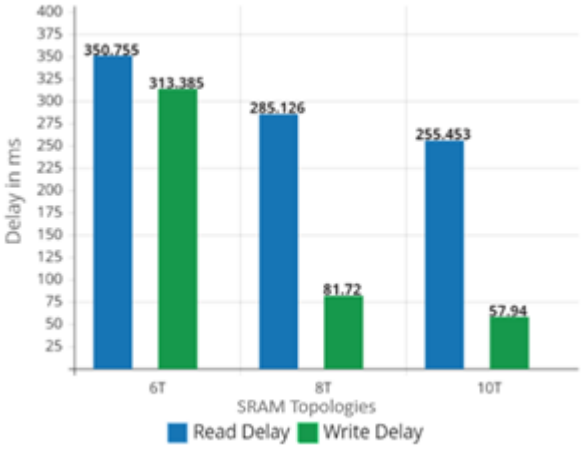

Fig 9: Comparison of Read and Write Delay

The Table.1 (Column 4 and 5) and Fig 9 shows the contrast between read and write delay of 6T, 8T and 10T SRAM Cells.

6T SRAM has a read delay 23.02% more than 8T SRAM and 37.31% more than 10T SRAM. Similarly, the write delay of 8T SRAM is 73.92% less than 6T SRAM and 10T SRAM has 81.51% less write delay than 6T SRAM. We observe that the read and write delay decreases as transistor sizing increases which indicates the increase in speed of SRAM cells with sizing.

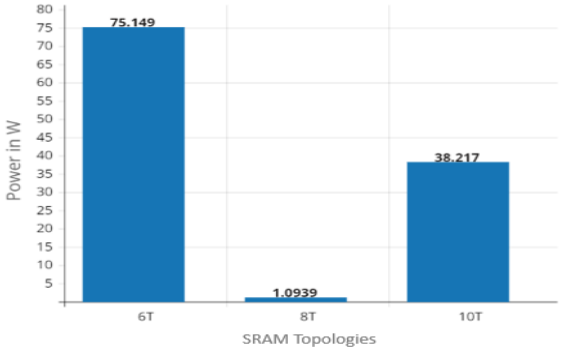

Fig 10: Comparison of Average Power

The Table.1 (Column 5 and 6) and Fig.10 illustrates the contrast between average power of 6T, 8T and 10T SRAM Cells. The average power of 10T is 45.01% less than 6T SRAM. It is also observed that it is less than average power of 8T SRAM. This indicates that 10T SRAM has less leakage power and is operating more efficiently when compared to other two SRAM cells. Fig. 11, 12, 13 shows the layout of the SRAM cells.

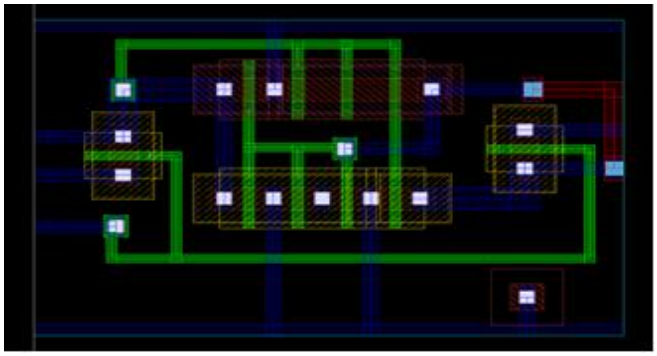

Fig 11: 6T SRAM Cell layout

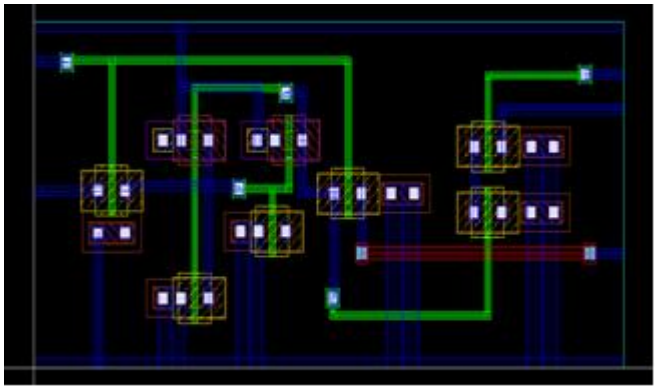

Fig 12: 8T SRAM Cell layout

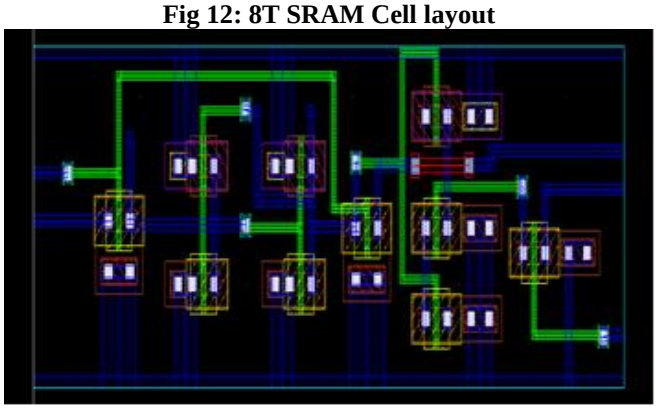

Fig.13: 10T SRAM Cell layout

IV. CONCLUSION

In this work standard 6T SRAM is compared with 8T and 10T SRAM cells in terms of read power, write power, read delay, write delay, and average power. 10T SRAM has the same range of read and write power. 6T SRAM has more write power and more delay compared to other SRAM. 6T is efficient in terms of read power but if we consider other parameters 10T SRAM cell is found to be more efficient compared to 6T and 8T.

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Ethical Approval and Consent to Participate	No, the article does not require ethical approval and consent to participate with evidence.
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Authors Contributions	All authors have equal participation in this article.

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