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Low Power CMOS Design of an SRAM Cell with Sense Amplifier

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Abstract: Power dissipation and switching delay are the focusing point in any circuit used in memory. It is required to design a circuit having low power dissipation and high switching speed in order to meet the current requirements. Reduction in power can be done by several methods. Here low power current sensing scheme for CMOS SRAM is presented in this paper. Large bit-line capacitance is one of the main bottlenecks to the performance of on-chip caches. New sense amplifier techniques need to explicitly address this challenge. The current sense amplifier senses the cell current directly and shows a speed improvement of 17-20% for 128 memory cells as compared to the conventional voltage mode sense amplifier

Index Terms: CMOS, SRAM, Sense Amplifier, Swithching delay, VLSI

I. INTRODUCTION

Memories are considered to be essential part of a system. Designer always try to reduce the amount of power dissipation associated with it. With increasing demand for battery operated applications, methods for reduction of the power consumption of the memory blocks have received significant interest. Six transistor SRAM cells are preferred for many applications because of its high speed and robustness [1]. If we increase dimension of SRAM then all other parameters such as, the leakage is becoming a growing concern. Besides, the leakage current increases with technology scaling, hence, dc power minimization has become a priority and been addressed by innovative solutions. To reduce the power and enhance the switching speed many approaches has been proposed. The critical issue of power and speed is resolved by utilizing a single ended pseudo differential circuit current sense amplifier [2]. Power can also be reduced by using hierarchical bit line and local sense amplifier [3]. In this paper a different scheme is proposed where current sense amplifier is used to reduce the power dissipation and improve the switching characteristics.

Generally speed, power and area are considered as the crucial point. One of the parameter can be achieved with compromisation of other two [4]. In this paper Section I covers background introduction, conventional 6T SRAM cell is discussed in section II, section III consists of proposed circuit and its description, results are presented in section V and finally section VI concludes the paper.

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II. CONVENTIONAL 6T SRAM CELL

Semiconductor memories can be broadly classified into two groups; read only memory and random access memory. The SRAM is fall into the category of random access memory, where the content of the memory can be accessed randomly. A graph of semiconductor memory organization is shown in figure 1. Memories can also be classified on the basis of access time, function and size. SRAMs basically come in two different flavors: synchronous and asynchronous. Synchronous SRAMs are devices that are synchronized with an external signal called a clock. The device will read and write information into the memory only on particular states of the clock. The particular state of interest is when the clock switches, i.e., when it goes from either LOW-to-HIGH ("rising edge"), or from HIGH-to-LOW ("falling edge"). An asynchronous SRAM, on the other hand, does not depend on the state of a clock. Memories are classified as semiconductor memories and magnetic memories. RAMs are of two types, static and dynamic. Circuits similar to basic **D** flip-flop are used to construct static RAMs (**SRAM**s) internally. A typical SRAM cell consists of six transistors which are connected in such a way as to form a regenerative feedback. In contrast to DRAM, the information stored is stable and does not require clocking or refresh cycles to sustain it. Compared to DRAMs, SRAMs are much faster having typical access times in the order of a few nanoseconds. Hence SRAMs are used as level 2 cache memory.

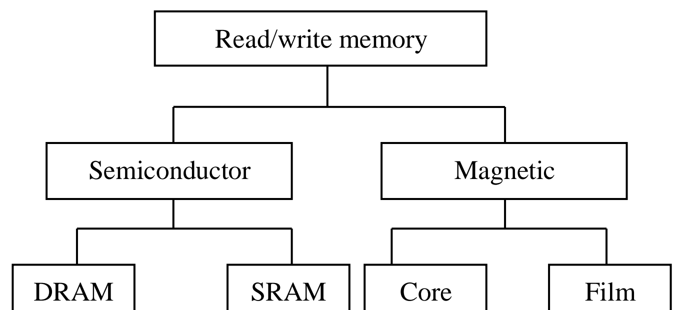

Figure 1. Memory Organization.

SRAMs have experienced a very rapid development of low-power low-voltage memory design during recent years due to an increased demand for notebooks, laptops, hand-held communication

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devices and IC memory cards.
The SRAM cell should be sized as small as possible to achieve high density in memory design. Figure 2 shows the conventional SRAM cell. Word line is used for enabling the access transistors M1 and M2 for write operation. BL and BL Bar lines are used to store the data and its compliment. For write operation one BL is High and the other bit line on low condition. For writing "0" BL is Low and **~BL** is high. When we assert the word line high transistor M1 and M4 is on and any charged stored in the BL goes through M1- M4 path to ground. Due to Zero value at Q the M5 transistor is ON and M6 is OFF so the charged stored at **~Q** line. Similarly in the write "1" operation BL is high due to this M6 is ON and the charge store on the **~Q** is discharged through the M2-M6 path and due to this low value on the M3 is ON and M4 is OFF so the charged stored on the Q. Simulated result of 6T SRAM is shown in figure2. Here we take supply voltage 1V and W/L is equal to 1.5.

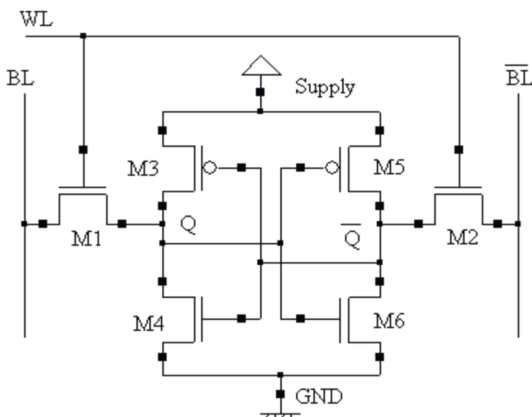

Figure 2. Conventional 6T SRAM Cell

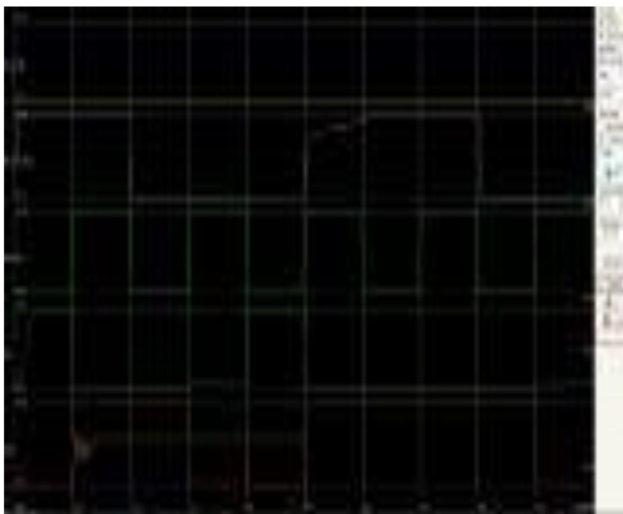

Figure 3. Simulated result

II. a SRAM operations: SRAM operate in three different states: stand by, reading, writing [5].

Standby: If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross coupled inverters formed by M1 – M4 will continue to reinforce each other as long as they are connected to the supply.

Reading: Assume that the content of the memory is a 1, stored at Q. The read operation is done by using the sense amplifiers that pull the data and produce the output. The row decoders and column decoders are used to select the appropriate cell or cells from which the data is to be read and are given to the sense amplifiers through transmission gate.

Writing: The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL bar to 1 and BL to 0. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters.

II. PROPOSED SRAM:

Schematic of proposed current sense amplifier shown in figure 4 used in the proposed scheme has a lower power consumption and a higher sensing speed than those of recently proposed. The sense amplifier mainly used to improve the switching speed of the SRAM. In convention SRAM due to large word-line capacitance the switching speed suffers, but when we use a sense amplifier the switching speed improve significantly. Two operating periods of the proposed SRAM are defined below.

III. a Equalizing period:

In equalization period, M6 and M9 turn off, small size transistor M7 and M8 are the load transistors of sense amplifier. Because of the high load resistance caused by the small size transistors, the DC current flowing through the sense amplifier is reduced. Since the sense amplifier dissipates little power in its sensing period, the whole power consumption of sense amplifier decreases apparently with the equalization current reducing.

IV. b Sensing period:

In sensing period, large size transistors M6 and M9 turn on so that the amplifier has a high current draining capability to enhance the sensing speed. In addition, the higher load resistance in equalization period conduces to constitute a bigger voltage difference between nodes C and D, which is caused by the differential current signals I1 and 12, at the beginning of sense operation. This is another speed enhancing factor for the proposed sense amplifier.

For proposed SRAM cell, the size of load device is the sum of M6 and M7, or the sum of M8 and M9.

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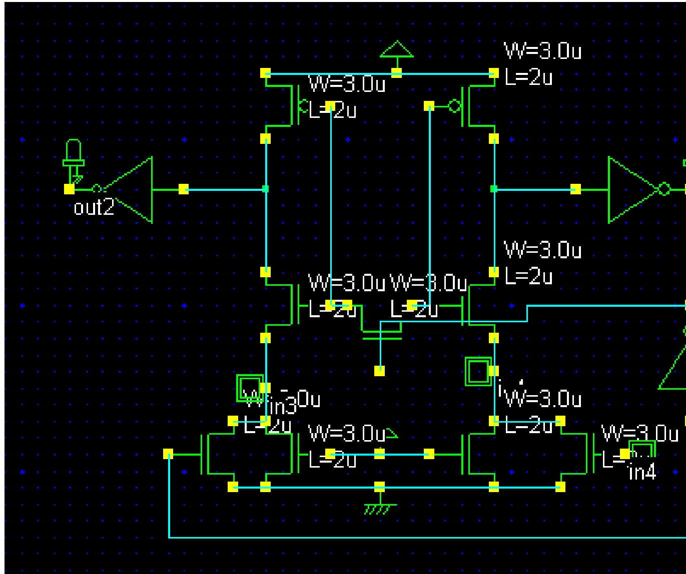

Figure 4.Schematic of Proposed SRAM cell

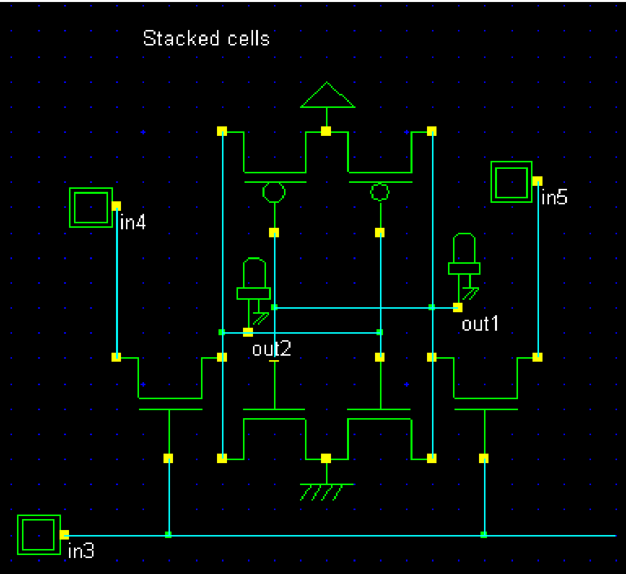

Figure 6 Schematic of .cross-coupled latch sense amplifier

III. c Circuit description: The circuit mainly consist a current sense amplifier. Current sense amplifier is special purpose amplifiers that output voltage proportional to the current flow. This architecture include current mirror cell that copy the current of bit-lines [6]. In conventional amplifier the output strongly depends on output voltage. The proposed sense amplifier improves the impedance compare to conventional sense amplifier. Conventional sense amplifier with cross-coupled latch is shown in figure 5 and schematic is shown in figure 6.

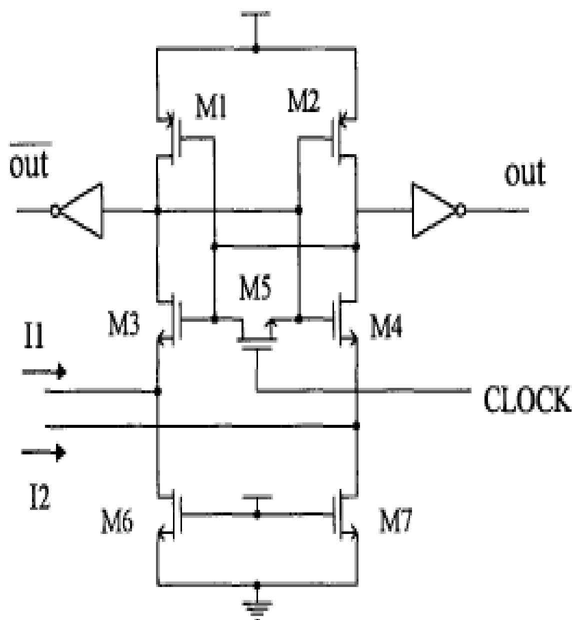

Figure 5 Conventional cross-coupled sense amplifier.

In conventional sense amplifier, the design of thesensor is based on the classical cross-coupled latch (M4-M7) and bit-line equalization (M1-M3). The operation of sense amplifierpresent in two common phases: precharging and equlizing.

IV. SIMULATION RESULT: The proposed current sensing scheme has been implemented based on **1.2 micro** CMOS technology and verified by HSPICE simulation. Shown in Figure 07 are the waveforms of simulation. The first illustration shows the ATD signal, column selector equalization signal EQ and the voltage changing of the internal nodes of the current mode column selector. The CLOCK signal and the output of sense amplifier are presented in the second picture. The switching of RS clock signal EN, SCDS and the output of RS latch are described in the third picture. With 4pf capacitive loads in both bit line and data line, the average current consumption of this current sensing scheme is 0.68mA. Under the same condition, the power consumption of the previous scheme is 0.87mA. Because the current sensing technique is employed in this scheme, the sensing delay is insensitive to both bit line and data line capacitances. The sensing delay (from CLOCK signal to the output of RS latch) with different bit line and data line capacitances is shown in Figure 08.

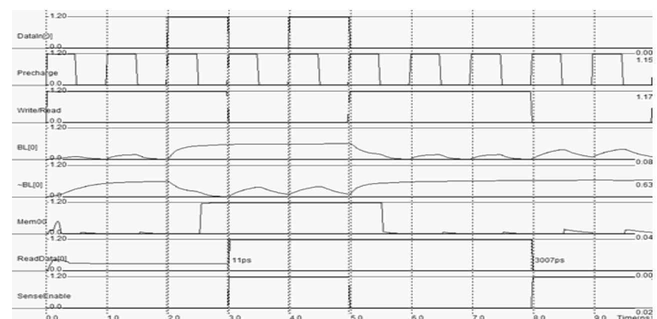

Figure 7. Simulated waveforms

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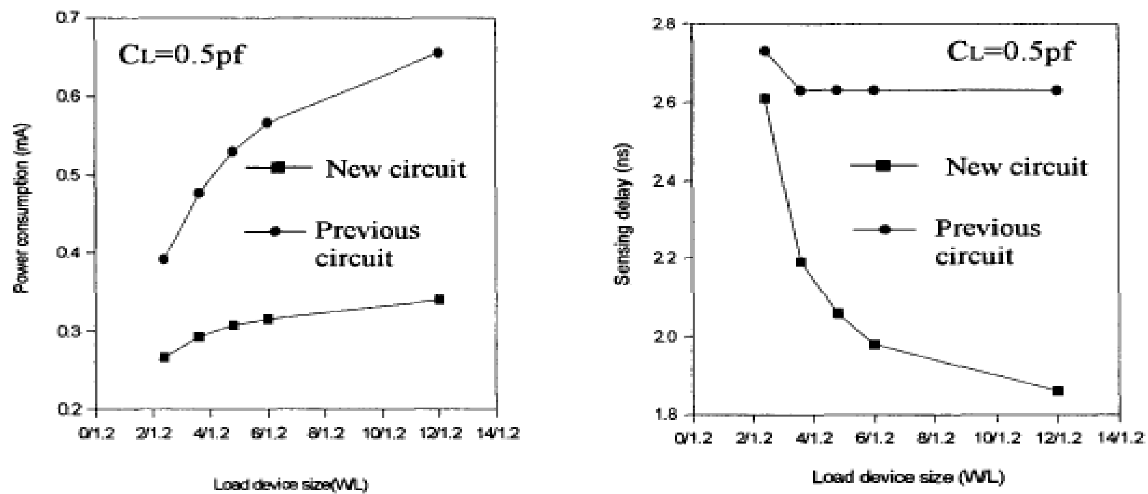

Figure 8. Power consumptions and sensing delay of the two current sense amplifier

CONCLUSION

In this work, efforts have been done to reduce the equalization current of cross-coupled latch sense amplifier. Because this equalization current is the main cause of static power consumption for this type of sense amplifier, this power saving step is effective. Some speed enhancement is also obtained by this measure. A clock control RS latch is introduced to screen out the untypical CMOS level output voltage of the sense amplifier, which usually causes the static power consumption in its following stage. A modification to the current-mode column selector is proposed to eliminate the unbalancing state between the internal nodes of MOS current conveyor after read operation. Employing above circuits, a low power current sensing scheme is developed. Its sensing speed is less than 3ns and insensitive to both bit line and data line capacitances.

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