International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-2 Issue-1, October 2012

Emulator for FPGA based RADAR signal processing

C. Thippeswamy, J. Chinna Babu, K. Padmapriya

Abstract-The present day RADARs use complex schemes such as stagger PRI, jitter PRI along with frequency agile characteris-tics. The frequency agile RADARs switch frequencies with in a pulse to get different types of advantages. Today lot of RADAR (Radio Detection and Ranging) signal processing takes place on FPGA(Field Programming Gate Array) platform.Th-se signal pr ocessing algor-thms include pulse parameters estimation, deint-e rleaving of mixed pulse patterns, processing complex chirp signals etc. All these algorithms need to be tested at various levels before they get integrated in to final system. However today no technique or solution available by which, these algoritms can be tested on FPGA with realistic signals. In this project a RADAR signal emulator will be built which can generate the samples even corresponding to multiple complex RADARs at a time. Since FPGA is a parallel platform this emulation is possible.

The complete project development consists of mainly two modules, the scenario creator and control logic. The control logic communicates with PC using serial port to capture the parameters set by the user in PC. These parameters are loaded into respective source simulator modules. Each source simulator module consists of NCO for digital carrier generation and pulse modulator. The NCO is programmable to generate all types of frequency agile signals in real time. A top level module consists of all these blocks and will be synthesized to Xilinx FPGAs. The final FPGA output will be demonstrated in real-time with Chip scope.

Keywords-RADAR, FPGA, PRI, Jitter PRI, Emulator.

I. INTRODUCTION

Radar parametric testing has traditionally required either expensive trials in real-world situations (with many uncontrolled variables) or very limited 'canned' tests. The Von Neumann processors normally used for signal processing are severely limited in this application because of the inherently serial instruction stream. This project work discusses the use of FPGAs to the processing to obtain a near real-time environment simulator. The FPGA logic handles the time sensitive tasks such as target sorting, waveform generation, sea clutter modeling and noise generation. DSP microprocessors handle the less critical tasks like target movement and radar platform motion. The result is a simulator that simultaneously produces several hundred independent moving targets, realistic sea clutter, land masses, weather, jammers and receiver noise. Traditional Radar Target Generators are built to test, debug, and demonstrate radar and target tracking functions.

Their aim is not a realistic simulation of the radar environment, but rather to perform some basic testing. The number of targets is limited and target motion is simple. The radar platform doesn't change position or attitude. Interference is simulated by a simple Gaussian noise generator. The test scenarios are canned; there is no real time interaction between the radar/operator and the Emulator. The Radar Environment Simulator is controlled by, and is partially implemented in software. Tasks that are not time critical are handled by software. Time critical tasks are performed by custom hardware.

II. SIMULATOR OR EMULATOR BASED RADAR SYSTEMS

Radar Emulator is the technique used test the various techniques or methodologies being developed for RADAR systems which can be tested without being cost-effective realistic radar systems.

The simulators have been developed for scholars or researchers in the field of Radar processing for its high performance to test its signal processing applications at software level to implements new ideas and method as far as the modulation schemes utilized. But at these simulators intended user may not get as précised output results and need to have a special system which replaces the following

(i) The output results as close to the practical values of realistic radar system and

(ii) Rapid development platform for emulator and cost effective

The Field Programmable Gate Array has been chosen because of the above mentioned reasons and is best suited one to make a Radar Emulator, which is mention above.

As far as the FPGA development is concerned it is a parallel platform and many number of signal generations can be done and tested simultaneously for Radar techniques which involves frequency agile characteristics like linear Frequency of non-linear frequency techniques, constant frequency or combination of all these.

III. DESIGN METHODOLOGY

The emulator design on FPGA RADAR based test processing applications may be described by the following design methodology. The modules identified for implementation in FPGA are Timing Generator, base band waveform generator, Upconvesion to IF, BITE generator and Direct Digital Synthesizer (DDS) programmer for frequency synthesis.

Manuscript published on 30 October 2012.
* Correspondence Author (s)
C.Thippeswamy*, ECE AITS, Rajampet, JNTU Anantapur, A.P, India.
Mr.J.Chinna Babu, Assistant Professor Department of ECE, AITS, Rajampet, JNTU Anantapur, A.P, India.
Dr.K.Padmapriya, JNTUCE, Anantapur, A.P, India.

The following diagram shows the simplified description of the RADAR Emulator Implemented on single FPGA board and for demonstration purpose we used a PC.

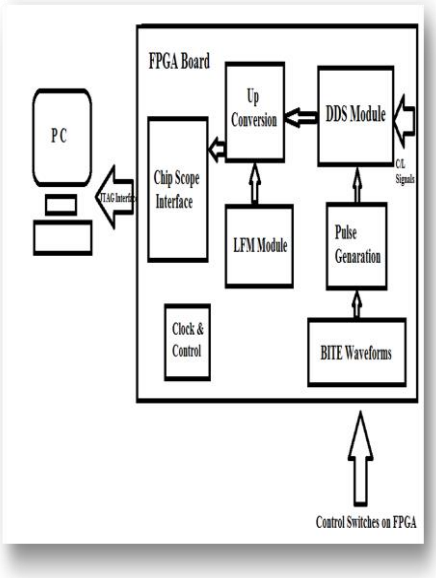

Figure1. Functional overview of RADAR Emulator Implemented on FPGA.

The functional modules shown above all the major blocks expect DDS (Direct Digital Synthesizer) has implanted by IP Core from Xilinx core generator tool and remaining are using VHDL. External control switches from FPGA development board has been used to get different combinations of frequency and an attenuation variation which resembles the phase and noise as added to original received echo signal from target as viewed in RADAR.

A. Waveform coefficient generation

The waveform coefficients are computed and stored in the ROMs of the FPGA. In this design, we consider the linear frequency modulation for the waveform. Frequency or phase-modulated waveforms can be used to achieve much wider operating bandwidths. Linear Frequency Modulation (LFM) is most commonly used [4]. In this case, the frequency is swept linearly across the pulse width, either upward (up-chirp) or downward (down-chirp).

The LFM up-chirp instantaneous phase can be expressed by $\Psi(t)= 2*\Pi*(f0 * t + \mu * t2 /2)$ $-\tau/2 \leq t \leq \tau/2$, where f0 is the radar centre frequency, and $\mu=2¶B/t$ is the LFM coefficient. Thus, the instantaneous frequency is $f(t)= (1/2*\Pi)* d/dt (\Psi(t))= f0 + \mu * t$ $-\tau/2 \leq t \leq \tau/2$, (2) Similarly, the down-chirp instantaneous frequency is given by $f(t)= (1/2*\Pi)* d/dt (\Psi(t))= f0 - \mu * t$ $-\tau/2 \leq t \leq \tau/2$, (3). The linear frequency modulation coefficients are computed as per above equations. The sampling frequency is chosen corresponding to the bandwidth of the waveform to be generated. These coefficients are computed offline for different pulse widths and stored into the ROMs of the FPGA. In real time these coefficients are read in the FPGA to generate LFM waveform at IF.

B.Up conversion of frequency modulated waveform to IF

Figure.2 shows the design schematics of up-conversion (to IF) module as implemented in FPGA.CPI, BITE, PRT signals from the input to the module along with the clock. These are the timing signals, which are generated in the FPGA from the external encoder data (explained previously). CPI is used to synchronize the modulated waveform with the radar timings. PRT acts as the cover pulse of the transmission waveform and is used to enable the DDS (Direct Digital Synthesizer) implemented in the FPGA. When enabled the DDS generates continuous wave signal at the IF at which LFM is to be generated.

So the DDS generates continuous wave at 40 MHz during the PRT. The complex continuous waveform at the output of the DDS is then multiplied with the LFM coefficients (at baseband) already stored in the ROM of the FPGA (as explained in previous section). There are two banks of ROMs, one for cosine LFM coefficients and other for sine LFM coefficients. The user* from the display selects the pulse width for which LFM is to be generated and the information is conveyed to the FPGA. According to the pulse width selected, the selection of ROM is done and the LFM coefficients are read out in real time to form the LFM waveform at IF. Accordingly, the ROM selection bits are set and address generation is done to read the coefficients from the ROM.

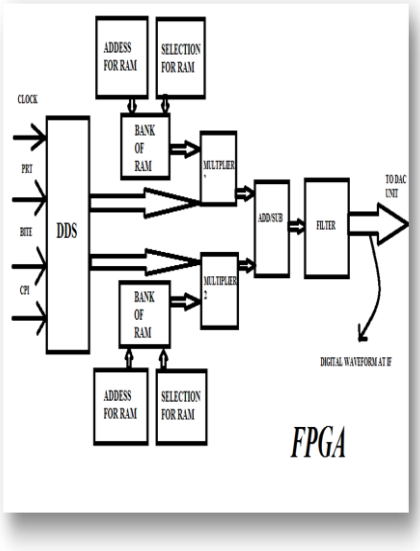

Figure2. Baseband Generation and Upconverion Unit

CPI is used to synchronize the modulated waveform with the radar timings. PRT acts as the cover pulse of the transmission waveform and is used to enable the DDS (Direct Digital Synthesizer) implemented in the FPGA. When enabled the DDS generates continuous wave signal at the IF at which LFM is to be generated.

So the DDS generates continuous wave .1MHz during the PRT. The complex continuous waveform at the output of the DDS is then multiplied with the LFM coefficients (at baseband) already stored in the ROM of the FPGA (as explained in previous section). There are two banks of ROMs, one for cosine LFM coefficients and other for sine LFM coefficients. The user from the display selects the pulse width for which LFM is to be generated and the information is conveyed to the FPGA.

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)

According to the pulse width selected, the selection of ROM is done and the LFM coefficients are read out in real time to form the LFM waveform at IF. Accordingly, the ROM selection bits are set and address generation is done to read the coefficients from the ROM.

After multiplication of the cosine and sine components of the continuous signal at IF with corresponding LFM coefficients, the signal at the output of the multipliers is subtracted to from the linear frequency modulated signal at the IF. The signal is then filtered by a band pass filter implemented in the FPGA so as to remove the out of band components. The digital LFM signal (at the IF) at the output of the FPGA is then fed to an external Digital to Analog Converter (DAC) followed by an analogue filter. The signal is then up converted to the desired transmission frequency by RF up converters and transmitted during the PRT pulse.

C. BITE waveform generation

BITE is used to check the essential functionalities of the radar when it's not transmitting. It acts as the echo return from real targets. Our design is capable of generating BITEs with and without doppler i.e. moving as well as stationary targets can be simulated. The signal BITE enables the DDS for the range position during which the echo is to be simulated and thus acts as the cover pulse for the BITE to be generated. BITE position and doppler of the BITE are programmable by the user. The maximum doppler for which the BITE can be generated depends on the PRF chosen by the user and is equal to PRF/2. The cosine and sine components of this signal are then multiplied with the corresponding LFM coefficients as read from the ROM (selected as per pulse width) and then the same process of up conversion follows.

D. Direct Digital Synthesis (DDS) core

Function generators have been around for a long while. Over time, these instruments have accumulated a long list of features. Starting with just a few knobs for setting the amplitude and frequency of a sinusoidal output, function generators now provide wider frequency ranges, calibrated output levels, a variety of waveforms, modulation modes, computer interfaces, and in some cases, arbitrary functions. The many features added to function generators have complicated their design and increased their cost. There is an opportunity for a radical re-design of the familiar function generator using direct digital synthesis (DDS).DDS provides remarkable frequency resolution and allows direct implementation of frequency, phase and amplitude modulation. These features which were 'tacked-on' to function generators now are handled in a clean, fundamental way by DDS.

The LogiCORE™ IP DDS (Direct Digital Synthesizer) Compiler core sources sinusoidal waveforms for use in many applications. A DDS consists of a Phase Generator and a SIN/COS Lookup Table. These parts are available individually or combined via this core. Direct digital synthesis (DDS) is a method of producing an analog waveform usually a sine wave by generating a time-varying signal in digital form and then performing a digital-to-analog conversion. Because operations within a DDS device are primarily digital, it can offer fast switching between output frequencies, fine frequency resolution, and operation over a broad spectrum of frequencies. With advances in design and process technology, today's DDS devices are very compact and draw little power.

IV. FPGA IMPLEMENTATION MODELS AND RESULTS

The paper emphasizes the implementation of the design using Field Programmable Gate Arrays (FPGA).The whole design explained above has been implemented on a single FPGA.

Our design implementation uses VHDL coding and Xilinx System Generator® (XSG) design tool to realize various functions. Waveform generation implementation model and upconversion models are designed using system generator. This model has been integrated with the VHDL modules to generate the bit file for programming of the Xilinx FPGA on a target board.

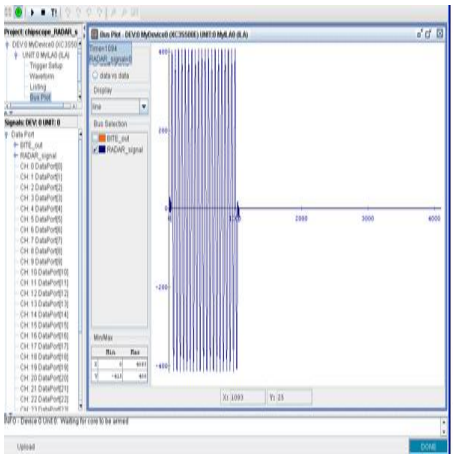

Figure3. RADAR waveform being observed at FPGA output

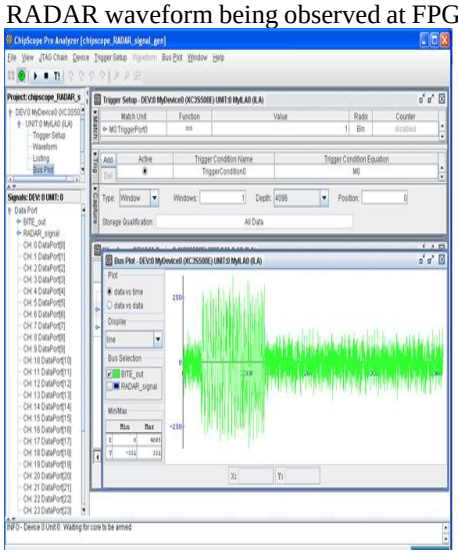

Figure4.BITE waveform being observed at FPGA output

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)

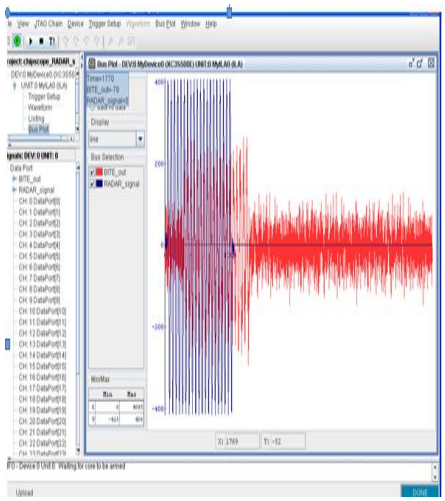

Figure5. RADAR and BIET waveforms being observed at FPGA output

Fig 3, Fig 4 and Fig 5 show the waveform generated by the FPGA as captured on Chipscope at the output of FPGA on board in radar.

This design has been used in ground based and ship based radars and performance in field has been up to expectations. This model can be used as a typical platform for academic and research scholars to develop and implement their ideas of new algorithms and method being developed for Radars systems with low cost.

V. CONCLUSIONS

Thus, the paper explains the digital methodology behind the realization of waveform generation. These digital methods facilitate the Radar signal generator with high degree of flexibility. In the digital waveform generation function based on the pulse characteristics and modulation schemes, the respective waveform code sample may vary. These samples will be stored in the respective memory modules. But this unique design model can be used for the generation of different radar waveforms for different radar systems. The utilization of the customized cores in the design models delivers high level of performance and area efficiency. Thus it resulted in an efficient implementation of the hardware using less percentage of FPGA resources. In addition, digital implementation is advantageous because the system becomes highly flexible, simple and reliable.

REFERENCES

1. *Byron Edde*, RADAR- Principles, Technology, Applications.
2. *Simon Kingsley, Shaun Quegan.*- Understanding Radar systems
3. *Merill Skolnik* - Introduction to Radar Systems, *2nd edition, McGraw Hill, 1980*
4. JR Klauder AC Price, S.darlington and WJalbersheim,"The Theory and Design of Chirp Radars" bell syst.tech j, volume 39pp745-808.
5. *Nadav Levanon and Eli Mozenson Radar Signals IEEE Press, Wiley Inter science 2004*

Thippeswamy.C has received his B.Tech in E.C.E in 2010 from KEC, Kuppam and currently pursuing his M.Tech in VLSI System Design from AITS, Rajampet, under the guidance of Mr.J.Chinna Babu. His field of interest includes Signal Processing and VLSI Design.

Mr.J.Chinna Babu has received his M. Tech degree in VLSI System Design. Currently, he is working as Assistant Professor in the Department of Electron-ics & Communicati on Engineering,AITS,Rajampet, Kadapa, A.P, and India. He has published a number of research papers in various National and International Journals and Conferences. His areas of interests are VLSI, Micro processor, Embedded Systems and Signals and Systems.

Dr.K.Padmapriya, Assistant professor in JNTUCE, Anantapur, A.P, India.

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)