International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-2 Issue-3, February 2013

Improved Natural Balancing Of Ripple Rejection LC-Filter with Modified Phase-Shifted PWM for Single-Leg Five-Level Flying-Capacitor Converters

Vijoy Kumar Peddiny, P.Swaminathan

Abstract*—Multilevel power electronic converters are the converter of choice in medium-voltage applications due to their reduced switch voltage stress, better harmonic performance, and Lower switching losses. Flying-capacitor multilevel converter has a distinct advantage in terms of its ease of capacitor voltage balancing. This paper analyses the natural voltage-balancing characteristic of a flying capacitor multilevel converter when it is operated under the spectrally modified Phase Shifted-pulse width modulation (PWM) strategy. Filter network connection is proposed that significantly improves the natural balancing response of a flying capacitor converter for either PWM strategy. This is most significantly done by simulation.

Keywords-Multilevel inverter, Phase shifted-PWM, Single leg five level Flying capacitor converter, self pre-charging.

I. INTRODUCTION

Multilevel converters have become a popular option in medium-voltage applications. While common two-level converters utilize direct series connection of switches to meet medium-voltage requirements, multilevel converters allow higher voltage handling capability with reduced harmonic distortion and lower switching power losses. Multilevel converters have been continuously developed in recent years due to the necessity of increase in power level of industrial applications, especially high-power applications, such as high-power ac motor drives, active power filters, reactive power compensation, and FACTS devices [2]. Better overall performance, including capacitor voltage balancing, can be achieved either by increasing the capacitor's size and cost or by increasing the switching frequency, which reduces the converter's efficiency [2]. Multilevel power electronic converters are the converter of choice in medium-voltage applications due to their reduced switch voltage stress, better harmonic performance, and lower switching losses. Although it has received little attention, the flying-capacitor multilevel converter has a distinct advantage in terms of its ease of capacitor voltage balancing. A number of techniques have been presented in the literature for capacitor voltage balancing, some relying on "self-balancing" properties. However, self balancing cannot guarantee balancing of capacitor voltages in practical applications.

Manuscript published on 28 February 2013.
***** Correspondence Author (s)
Prof.P.Swaminathan, BE-EEE, M.TECH.-HVE, MBA-HR,[PhD-HVDC],,He has obtained his Degrees from MADRAS University, SASTRA University, PERIYAR University and with ANNA University, Tamilnadu, INDIA
Vijoy Kumar Peddiny,born in arunachal pradesh,received B.E degree in electrical and electronics engineering from Dr.Babasaheb Ambedkar marathwada university,Aurangabad Maharastra ,India

Other researchers' present closed-loop control schemes which force voltage balancing of capacitors. In this paper, a new closed loop control scheme is proposed which regulates the capacitor Voltages for a multilevel flying capacitor converter [3]. The flying capacitor converter (FCC) was introduced as a viable multilevel converter topology. Although the FCC topology is not as common as other structures, it has some distinct advantages over the diode-clamped topology including the absence of clamping diodes and the ability to regulate the flying-capacitor voltages through redundant state selection even if the number of voltage levels is greater than three. Different methods have been introduced in the literature to maintain capacitor voltage balancing. The simplest approach is to rely on the "self-balancing" property of the FCCs.

II. FIVE LEVEL FCC BALANCING TOPOLGY AND SWITCHING OPERATION

The topology of a five-level single-leg FCC are consist of four pairs of complementary controlled switches (S1 , Sc1), (S2 , Sc2), (S3 , Sc3), and (S4 , Sc4) Fig. 1.These switches make it possible to connect the flying capacitors in series with the load. The load is represented as RL series connection, to a simple inductive load. The flying capacitors C1, C2 and C3 should be charged to their nominal voltages Vdc/4, Vdc/2, and 3Vdc/4, respectively, to be able to construct the desired output voltages. To ensure that the voltage stress over the switches is limited and the output voltage quality is acceptable, the capacitor voltages need to remain nominal.

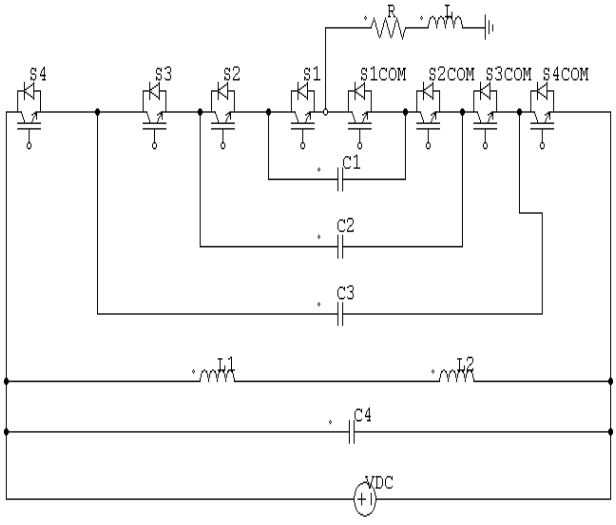


Fig. 1.Single Leg Five Level Flying Capacitor Converters

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)

III. CIRCUIT AND MODES OF SWITCHING OPERATION

FCC switching states consist of six circuit topology for zero voltage over load and Switch states 1 (1c2c34) and 2 (1c2c34)(Fig.2) can be considered as the inverse of each other, as are switch states 3 and 4 and switch states 5 and 6. The same current direction in these inverse circuits has an opposite effect on the capacitor voltages.

TABLE I

Switch states and the corresponding output voltages of a five-level single-leg FCC (when VC 1 = Vdc /4, VC 2 = Vdc /2 and VC 3 = 3Vdc /4)

List	Switch state	Vo
1	1c2c34	0
2	123c4c	0
3	12c3c4	0
4	1c234c	0
5	1c23c4	0
6	12c34c	Vdc/4
7	1c234	Vdc/4
8	12c34	Vdc/4
9	123c4	Vdc/4
10	1234c	-Vdc/4
11	12c3c4c	-Vdc/4
12	1c23c4c	-Vdc/4
13	1c2c34c	-Vdc/4
14	1c2c3c4	Vdc/4
15	1234	Vdc/2
16	1c2c3c4c	-Vdc/2

Circuit topologies of a five-level single-leg FCC resulting in zero load voltage. (a) Topology 1: 1c2c34. (b) Topology 2: 123c4c. (c) Topology 3: 12c3c4. (d) Topology 4: 1c234. (e) Topology 5: 1c23c4. (f) Topology 6: 12c34c. The four circuit topologies of a five-level FCC resulting in a load voltage of Vdc/4 are depicted in Fig. 3. The inverse of these switch states results in a load voltage of −Vdc/4 and corresponds with switch states 11–14. The two remaining possible switch states 15 and 16, which result in an output voltage of Vdc/2 and −Vdc/2, respectively, are created by closing all upper or bottom switches (1234 and 1c2c3c4c). As no flying capacitors are connected in switch states 15 and 16, their voltages are not altered and they do not have any influence on the load voltage.

IV. CARRIER PS-PWM OF FIVE LEVEL FCC FOR NATAURAL BALANCING

The most convenient way to control the capacitor voltages of an FCC is by using a modulation strategy, which results in natural balancing. This passive control method does not need measurements and the control effort is low. To achieve natural balancing, all the switch pairs in a phase leg must be controlled using the same duty cycle. The carrier is phase shifted over 2π/N-1 for an N-level converter. Each switch pair has their own triangular carrier wave. When D is above the carrier, the upper switch is closed and when below the carrier, the bottom switch is closed. The order of the carriers (here c1, c2, c3, c4, lead order) can be reversed to the lag order (c4, c3, c2, c1), without influencing the balancing time constants .The PS-PWM for five-level single-leg FCCs has been heavily analyzed mostly in the frequency domain. The time-domain analysis clarified that the voltage balancing is driven by the losses caused by current harmonics, which are generated by the unbalance of the capacitors. All loss mechanisms influence the dynamics of the voltage balancing. In this study, only the ohmic loss mechanism in the load is considered, but every additional loss mechanism speeds up the balancing dynamics. The time-domain analysis of the voltage balancing of the flying capacitors results in closed-form solutions of the time constants of the balancing dynamics. The obtained equations show the dependence on the system parameters (including load parameters) and D. The switch state sequence for D = 0is 1–3–2–4 (see Fig. 2 and Fig. 3).it is shown that the cause of this infinite time constant for D = 0 is found in the circuit topologies 1, 2, 3, and 4. It is clear from these topologies, see Fig. 2, that capacitors C1 and C3 are, for D = 0, always used as a pair and are always connected in an anti series way. If capacitors C1 and C3 both have the same voltage deviation, it is impossible to balance it out, as this unbalance has no influence on the output voltage. Besides this practical explanation, this can also be confirmed by theoretical reasoning. The balancing dynamics can be mathematically simplified by assuming Vdc = 0, ideal switches (no diodes), and charged flying capacitors. For a five-level converter, this is not only the case for ranges, where the flying capacitors are not used (*D* close to 1 and −1), but also for *D* close to zero. As an example, the balancing after a dc-bus voltage step for the PS-PWM with *D* = 0 is depicted. The easiest technique to control the flying capacitor voltages is natural balancing , achieved by switching the two-level cells within each phase leg at approximately the same duty cycle, but phase shifted by $2\pi/(N-1)$ is implemented using phase-shifted carrier (PSC) pulse width modulation (PWM) Fig 4 [5]. Natural balancing using (PSC) PWM is quite ineffective. Phase disposition (PD) PWM for multilevel converters, shown in Fig. 2(b), is known to be a superior modulation strategy, since it generates substantially lower levels of harmonic distortion in the switched output waveform. [5]

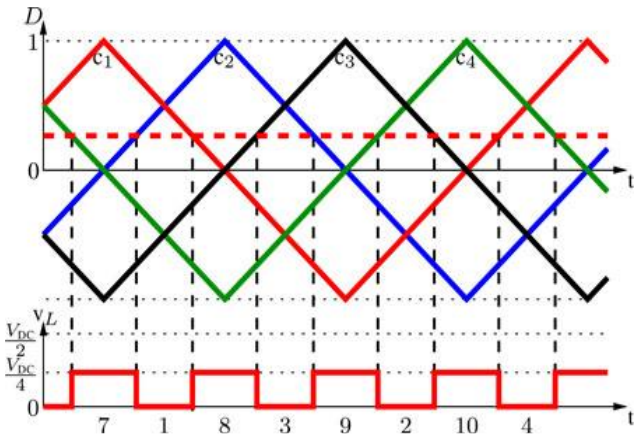


Fig. 2. Carrier Ps-Pwm of Five Level Fcc

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)

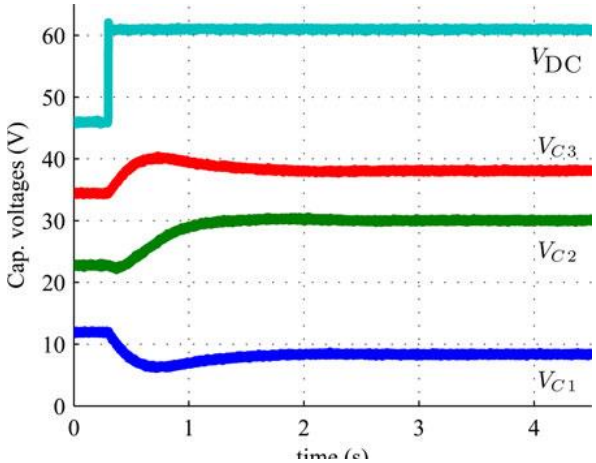


Fig.3. Carrier Ps-Pwm Of Five Level Fcc

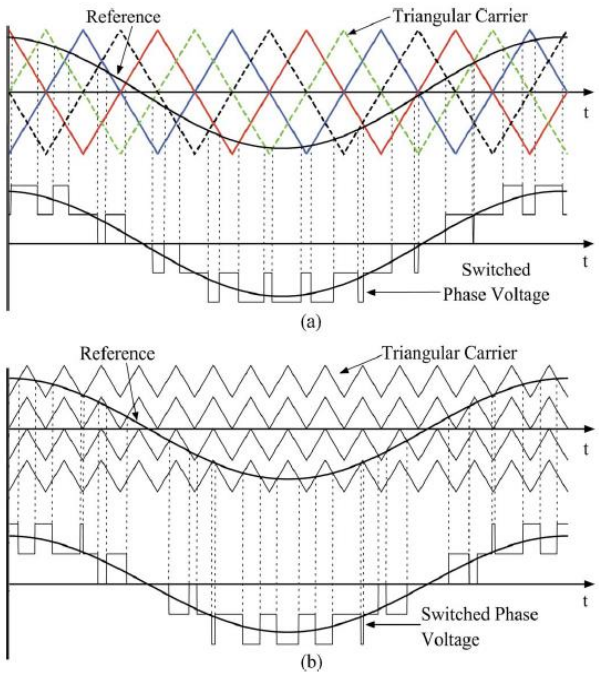


Fig. 4. Carrier Ps-Pwm of Five Level fcc

V. MODIFIED PS-PWM BALANCING CARRIER WAVE

The balancing aspects of a five level single-leg FCC, it was found that all switch states resulting in zero output voltage are necessary to guarantee a fast balancing. Other aspects that should be met are as follows.

1) Switch to the nearest levels to obtain the optimal voltage quality.
2) Consecutive switch states should differ only in the state of one switch (limit the switching losses).
3) Uniform distribution of the switching losses over the switch pairs.
4) Inverse states should be applied during equal time period. These elements will be implemented in a new modulation scheme with improved natural-balancing dynamics.
5) LCL filter rejection ripples distortion and reduces the harmonics noise.

VI. PS-PWM STRATEGY RELATED SEQUENCES

The proposed method of creating the modified PS-PWM sequences results in 72 possible sequences. These sequences are not all unrelated, in fact, most of them are related. This means some sequences can be created by a transformation of another sequence. These related switch-state sequences cannot only be constructed from each other, but their balancing dynamics are also related. Using these properties, the number of sequences that have to be investigated to find the optimum sequence can be significantly reduced. There are three ways to relate the sequences with each other. All three ways cause the number of sequences to be divided by 2. In the end, only three sequences for every base pair remain unrelated. The three ways to relate the sequences are discussed as follows. 1) Reversing the sequences: The sequences, which have the reversed order, result in the same dynamic parameters (the same time constants and oscillation frequencies). The only difference is a sign change of the sinusoidal term in the solution similar to the PS-PWM.Examples is 3–1–4–2–3–5–4–6 and 6–4–5–3–2–4–1–3. 2) Swap first and last part: Swapping the first four and last four states, 3–1–4–2–3–5–4–6 results in the same sequence as 3–5–4–6–3–1–4–2. 3) Mirror equivalent sequences: As can be derived from the carrier representation of Fig. 5, the sequence for D >0 is significantly different from the one for D < 0. This means that he balancing dynamics are also different for the two cases and not symmetrical around D = 0.

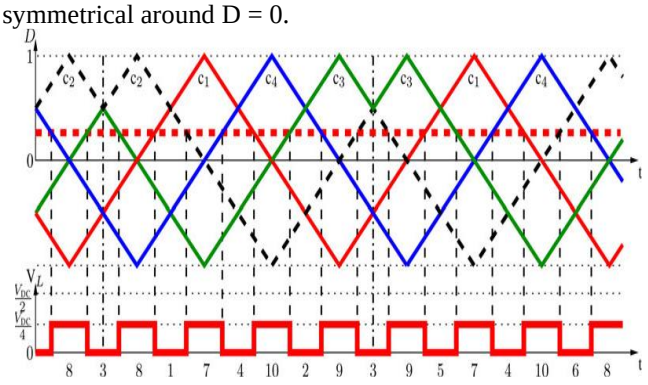


Fig. 5. . Modified Ps-Pwm Balancing Carrier Wave

VI. SELF PRE-CHARGING

The Precharging of an FCC is an important factor. In it is shown that using a ramp-controlled dc-bus voltage, while maintaining a zero average load voltage (D = 0) and a fast enough balancing, it is possible to apply self-precharge. This self-precharge is only applicable when the load is known, so the dc-bus voltage ramp can be adapted to the largest time constant of the balancing dynamics. For a five-level single-leg FCC, however, the normal PS-PWM is not appropriate as the time constant is infinite at the desired output voltage (D = 0). The modified PS-PWM scheme allows fast balancing at D = 0. The model that will be developed for the capacitor voltage balancing depends on the fact that vC1 < vC2 < vC3. If this is not the case, the clamping diodes of the switches are activated, introducing nonlinearities in the system.

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication (BEIESP)

In the self- precharge process, the capacitor voltages all start from 0 V, meaning that due to the balancing dynamics, the clamping diodes will interact with the balancing. It can be shown, however, that the effect of the clamping diodes reduces the balancing duration. The phase shifted sinusoidal PWM (PS-SPWM) method is considered an effective control method for the multilevel FCC since it benefits from self-balancing property when applied to an ideal and symmetrical circuit. Compared to other PWM methods, it is easier to balance the capacitor voltage in a relatively short time. However, to obtain voltage balancing, switching cells have to operate at the same duty cycle, the power devices must have the same characteristics, and the load current has to be symmetrical. Satisfaction of these conditions may not be guaranteed. Recently, several voltage balancing strategies have been presented which are based on the combination of the PS SPWM method with external control loops. These include methods which modify the duty cycles, choose different switching states, and add auxiliary voltages [4].

VII. BALANCING DYNAMICS AND SIMULATION

The voltage-balancing dynamics of a five-level single-leg FCC using PS-PWM was previously carried out in the time domain. The method for analyzing the balancing dynamics uses an averaged state-space model that is obtained by applying some assumptions. These assumptions are large enough capacitor values (to be able to neglect capacitor voltage changes during a PWM period) and an inductive load, which means that load time constant L/R is significantly larger than the PWM period. In practical terms, this means that the current ripple is low and can be considered as piecewise linear. The analysis of this averaged state-space model, where high-order terms are neglected, results in a general solution with time constants and oscillation frequencies. This method is directly applicable to the proposed sequences of the modified PS-PWM. For the analysis, the deviations of the capacitor voltages from their nominal (balanced) values are used. These are defined as

$$V_{d1} = V_{c1} - \frac{Vdc}{4}$$

$$V_{d2} = V_{c2} - \frac{Vdc}{2}$$

$$V_{d3} = V_{c3} - \frac{3Vdc}{4}$$

Where Vc1, Vc2, and Vc3 are the voltages of the flying capacitors C1, C2, and C3, respectively.

Dynamics system parameters

D	$-1<D<-0.5$	$-0.5<D<0$	$0<D<0.5$	$0.5<D<1$
$\frac{T_A}{K_T}$	$\frac{1}{(1+D)^2(1-2D)}$	$\frac{4}{5+6D}$	$\frac{4}{5+6D}$	$\frac{1}{(7+2D)(1-D)^2}$
$\frac{T_P}{K_T}$	$\frac{16}{(1+D)^2(13-32D)}$	$\frac{16}{15+6D-27D^2-16D^3}$	$\frac{16}{15+6D-27D^2+16D^3}$	$\frac{16}{(37+32D)(1-D)^2}$
Ω	$\frac{(1+D)^2 T_{PWM}}{16LC}$	$\frac{(1-2D^2) T_{PWM}}{32LC}$	$\frac{(1-2D^2) T_{PWM}}{32LC}$	$\frac{(1-D)^2 T_{PWM}}{16LC}$

The parameters of both presented modified PS-PWM sequences and the regular PS-PWM as a function of D. In the normalized time constants τA and τP are depicted Fig. (a) With as reference the minimum periodic time constant of PS-PWM. Fig. 6(c) shows the normalized oscillation frequency. The most significant difference between the PS-PWM and the modified PS-PWM sequences is noticeable in the aperiodic time constant. The infinite time constant for D = 0 has disappeared and the aperiodic balancing is faster over the full D-range. The aperiodic time constant Fig. 6(b). The periodic time constants of the modified PS-PWM sequences are slightly asymmetric and smaller than the periodic time constant of the normal PS-PWM. In general, the periodic time constant is smaller than the periodic time constant. The oscillation frequencies are equal for the PS-PWM and the first example of the modified PS-PWM. The oscillation frequency of the second example is these oscillation frequencies are of smaller interest in this study. They are a parameter of the step response, but have no real influence on the stability or the speed of the balancing. A sequence of the improved PS-PWM is not equally beneficial over the total D-range, especially because of the asymmetry. This can be overcome by using, in the example of sequence 1, For D < 0, the mirror equivalent sequence, while keeping the original sequence 1 for D >0. This results in symmetric be-haviour.

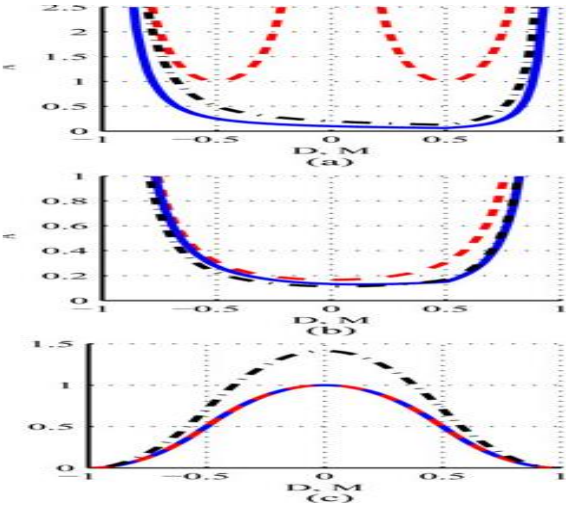
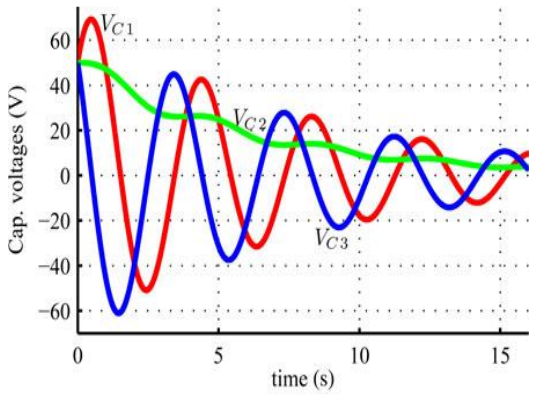


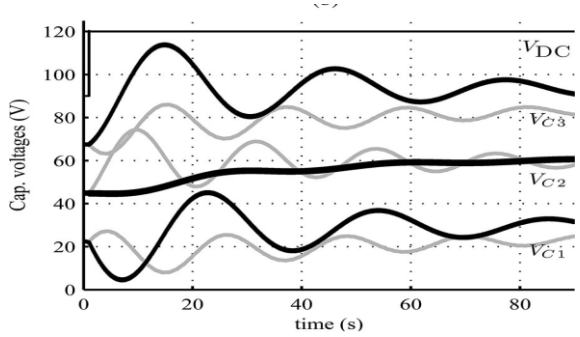
Fig. 6 (a) periodic time constant (b) aperiodic time constant(c) oscillation time constant

A. Simulation of voltage balancing initially charged capacitors=0 and zero DC Voltage



B. Simulation of voltage balancing across capacitors with D=0.2 and Vdc=90

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)



C. Simulation across load RL

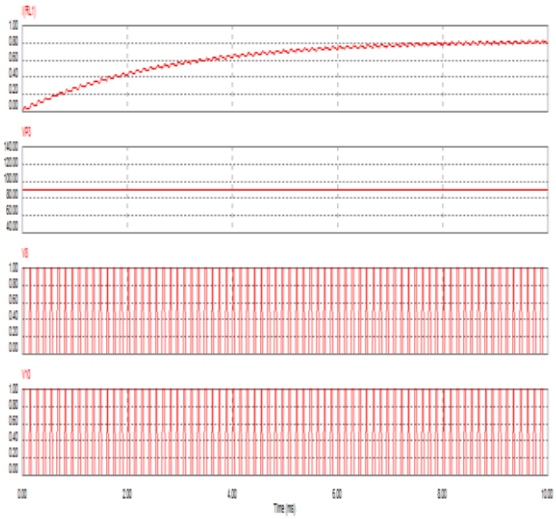
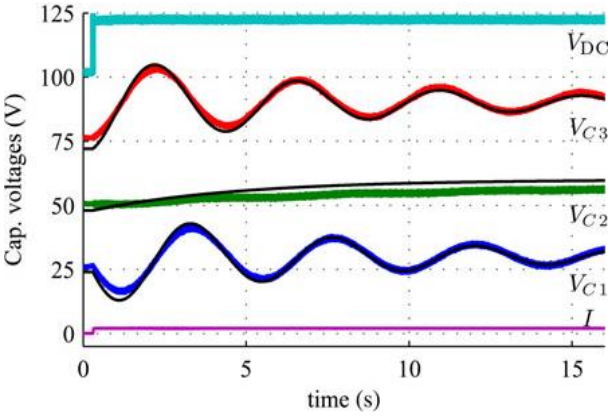


Table II

System parameters	Values
C1,C2,C3	1000uf(35v)
R	12ohm
L	12mh
L1	16mh
C1	1000uf
Vdc	60-90v
Switching frequency	750khtz

VIII. HARDWARE IMPLEMENTATION

The experimental hardware setup is a five-level flying-capacitor converter constructed half-bridge power electronic building blocks. The system parameters of the setup are given in the table. The converter is controlled with a Xilinx VirtexII-Pro FPGA (XUPV2P-30), clocked at 100 MHz or otherwise PIC controller processor used. An ironless choke is used as load to connect between the output and the mid-point of the voltage supply. A simple series connection of a resistance *R* and an inductance *L* is used as a model for the load. A LCL connection for better response of supply in the input supply and get output proper result. Because of the absence of an iron core, the parameters do not depend very much on the frequency. The inductance, as well as the resistance, is only slightly influenced by the frequency and taken constant. The load parameters are found using an LCR meter and multimeter.



Experimental hardware simulation with D=0.25 and Vdc=45v to 60v at t=0.3s

IX. CONCLUSION

Natural balancing of FCCs can be achieved by using the normal PS-PWM scheme. It was observed that the balancing is not guaranteed at certain regions of the duty ratio. For five level single-leg converters, there is no balancing for $D = 0$. A new PWM scheme should enhance the voltage balancing, while maintaining the optimal voltage quality of nearest voltage level switching and an equal distribution of the switching losses over the switches. The modified PS-PWM scheme creates 72 possible sequences, which are all related to nine original sequences, with their own balancing dynamics. Modified PS-PWM enhances 16 possible switches respective of system. This results in a reduction of the cost and size of the flying-capacitor-based converters and makes them more practical. These achievements are obtained by adding one cell, including one dc voltage source whose voltage rating is a small fraction of the main dc-link voltage rating, and two low-power high-frequency switches.

REFERENCES

[1] A. Shukla, A. Ghosh, and A. Joshi, "Hysteresis modulation of multilevel inverters," IEEE Trans. Power Electron., vol. 26, no. 5, pp. 1396–1409, May 2011.
[2] A. K. Sadigh, S. H. Hosseini, M. Sabahi, and G. Gharehpetian, "Double flying-capacitor multicell converter based on modified phase-shifted pulse width modulation," IEEE Trans. Power Electron., vol. 25, no. 6, pp. 1517–1526, Jun. 2010.
[3] F. Defay, A. M. Llor, and M. Fadel, "Direct control strategy for a four level three-phase flying-capacitor inverter," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2240–2248, Jul. 2010.
[4] M. Khazraei, H. Sepahvand, K. Corzine, and M. Ferdowsi, "A generalized capacitor voltage balancing scheme for flying-capacitor multilevel converters," in Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo., Feb. 2010, pp. 58–62.
[5] B. P.McGrath and D.G.Holmes, "Enhanced voltage balancing of a flying capacitor multilevel converter using phase disposition (PD) modulation," IEEE Trans. Power Electron., vol. 26, no. 7, pp. 1933–1942, Jul. 2011
[6] Vahid Dargahi, Arash Khoshkbar Sadigh, "Flying Capacitors Reduction in an Improved Double Flying Capacitor Multicell Converter Controlled by a Modified Modulation Method," IEEE Trans. Power Electron., vol. 27, NO. 9, Sep. 2012.
[7] A. Ruderman and B. Reznikov, "Five-level single-leg flying-capacitor converter voltage balance dynamics analysis," in Proc. IEEE 35th Annu. Conf. Proc. Ind. Electron., Nov. 2009, pp. 486–491.

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication (BEIESP)

[8] S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Self-precharge for single-leg odd-level multilevel converter," in Proc. IET 5th Int. Conf. Proc. Power Electron., Mach. Drives, Apr. 2010, pp. 1–6.
[9] R. H.Wilkinson, T. A. Meynard, and H. du Toit Mouton, "Natural balance of multicell converters: The general case," IEEE Trans. Power Electron., vol. 21, no. 6, pp. 1658–1666, Nov. 2006.
[10] Thielemans, A. Ruderman, and J. Melkebeek "Flying capacitor multilevel converter voltage balance dynamics for pure resistive load" in Proc. IET 5th Int. Conf. Proc. Power Electron., Mach. Drives, Apr. 2010.

Prof.P.Swaminathan, BE-EEE, M.TECH.-HVE, MBA-HR,[PhD-HVDC],,He has obtained his Degrees from MADRAS University, SASTRA University, PERIYAR University and with ANNA University, Tamilnadu, INDIA. His research area includes HVDC, VSC-HVDC, FACTS, AC DRIVES and RENEWABLE ENERGY. Presently he is working with department of EEE in KARUNYA University, Coimbatore, Tamilnadu, INDIA.

Vijoy Kumar Peddiny, born in arunachal pradesh,received B.E degree in electrical and electronics engineering from Dr.Babasaheb Ambedkar marathwada university,Aurangabad Maharastra ,India.Now currently doing M-tech in Power Electronics and Drives from Karunya university,coimbatore,India.