International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-2 Issue-3, February 2013

3-bit R-2R Digital to Analog Converter with Better INL&DNL

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Abstract— In this paper analysis of 3-bit R-2R ladder DAC proposed with most of the specification in the last decade has been done. All analysis have been supported by simulations results. To carry out the simulations Eldo spice, IC Station and Design architect from Mentor Graphics Tools is used. For all about Pre Layout simulation has been realized using (0.35um) CMOS process Technology.

IndexTerms—digital-to-analog converters(DAC),R-2R ladder network., DNL,INL

I. INTRODUCTION

Among the most popular architectures are DACs based on current steering and resistor ladders. These architectures are very well suited for implementation in standard CMOS processes and provide a good compromise between occupied area, power consumption, and speed. In general, requiring N-bit DAC resolution implies achieving an error of less than 0.5 LSB. Depending on DAC architecture, this translates to a maximum error of the MSB value (current or resistance).

II. R-2R LADDER NETWORK

The R-2R ladder consists of two different resistors placed in a configuration as shown in fig1.The inputs to the ladder are fed from a N bit inputs. The input voltages range from 0V to 2V. Here R-2R network is also converted in to the CMOS equivalent circuits. This configuration consists of a network of resistors alternating in value of Rand 2R. Starting at the right end of the network, notice that the resistance looking to the right of any node to ground is *2R*. Each node voltage is related to V_{ref} , by a binary-weighted relationship caused by the voltage division of the ladder network. The total current flowing from *Vref* is constant, since the potential at the bottom of each switched resistor is always zero volts. Therefore, the node voltages will remain constant for any value of the digital input. The output voltage, *Vout'* is determined by the equation 1[2].where D indicate the digital input word decimal value, n indicate DAC resolution, and DAC reference voltage is $V_{ref.}$

$$Vout = D \times (\frac{V_{ref}}{2^n}) \qquad (1)$$

Manuscript published on 28 February 2013.
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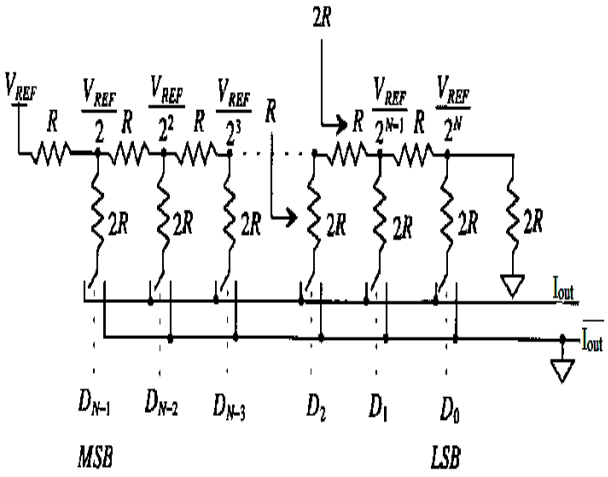

Fig.1 R-2R ladder DAC

III. CMOS EQUIVALENT CIRCUIT OF 3-BIT R-2R DAC

An example of a 3 -bit R-2R MOS converter is shown in figure2. In this figure R-2R cell shown with a possible combination with the bit current switch. All transistors in this system are equal.

Depending upon the input current 2I, transistor M1 and M2 divide the input current 2I.Transistors M1 and M2 can operate in saturated mode or in a triode mode. In saturated mode transistors M1 and M2 divide the input currents 2I in to two equal currents I. in this case transistor M3 acts as a cascade transistor and supplies the output currents to the load.

At the moments transistors m1 and M2 are in triode region, then these transistors can be seen as a resistor with value R. in this case transistor M3 performs an equal resistor of value R. in this way R-2R network is implemented and with careful termination an accurate binary weighted current division is obtained[4].

However it is possible to include the switches in to the network by adding transistor M4.at the moment data is high, then transistor M3 is used in the network as described before and the output current Iout = I1 is supplied to the load . at the moment data bar is high, then transistor M4 is used in the network as described before and the output current Iout Bar = I2 is supplied to the load.

By cascading method the basic elements of 3-bit converter can be designed as shown in fig 2[4]. the transistor system can be scaled depending upon the current value owing through the individual stages. In this system trail current 8I is divided by 4I, 2I, I and I .the extra current I is obtained in the last stage Is supplied to the bias voltage and it is not required for the digital to analog converter.

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With large size of the division transistor, it is possible to obtain 10 bit resolution with +/-0.5 linearity[1],[2]. An accurate switching of the current is required to obtain a small glitch when the digital to analog converter is switched around the MSB values .in the offset binary coded converter system. Timing is very important here. Biggest problem in R-2R DAC is mismatching of resisters values. This creates error in resolution. Resolution can be achieved by using operation amplifier or Low pass filter as a next stage. Proper switching is also very important.

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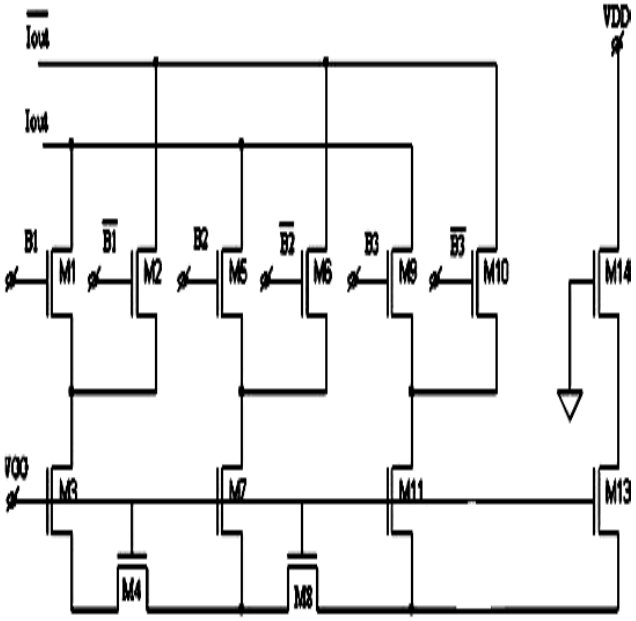

Fig.2 CMOS equivalent circuit of 3-bit R-2R DAC

Then to calculate the value of Resister related to different parameter is as follows, The resistance of a MOSFET operated in the linear mode is given by:

$$R = \frac{V_{DS}}{I_D} \qquad (2)$$

Where, V_{DS} = drain-source voltage, I_D= drain-current
The drain-source voltage and the drain current are related by:

$$I_D = \mu.C_{ox} \times (\frac{W}{L}) \times (V_{gs} - V_t) \times V_{ds}, \text{ for} V_{ds} < (V_{gs} - V_t)$$

IV. SIMULATION RESULT

By applying input volts=2.0v as a pulse and digital input from 000 to 111 for three bit we achieved respective voltage as shown in fig.3 and fig.4 and observe respective parameters like INL,DNL,Offset,etc.

A. Integral Nonlinearity

Here for 3 bit R-2R DAC input bits are from 000 to 111. And Y axis of fig.5 shows ideal and actual INL. Offset error must be corrected otherwise it will be replicated in all stage as INL errors.

We can find the values of INL by this way INL = Output value for input code n - Output value of the reference line at that point.

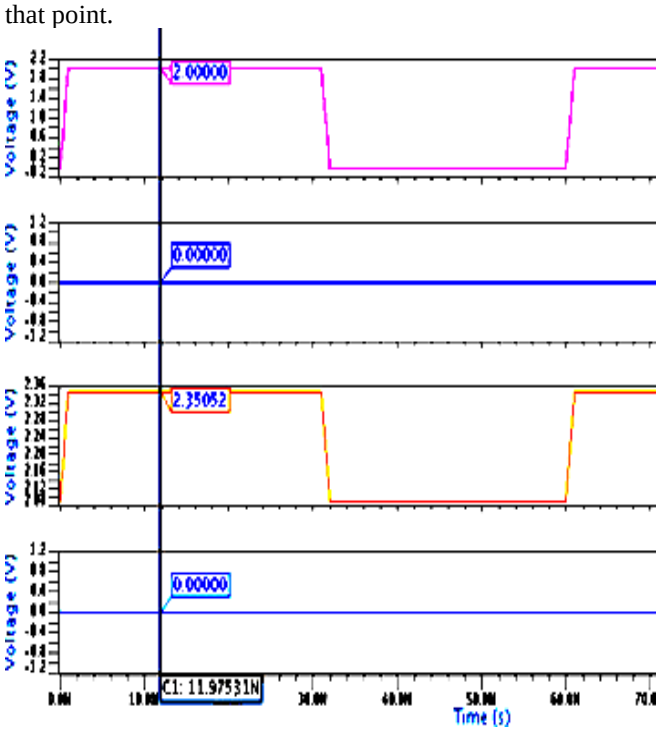

Fig.3 input 001 and output is 0.35V for 3 bit R-2R DAC

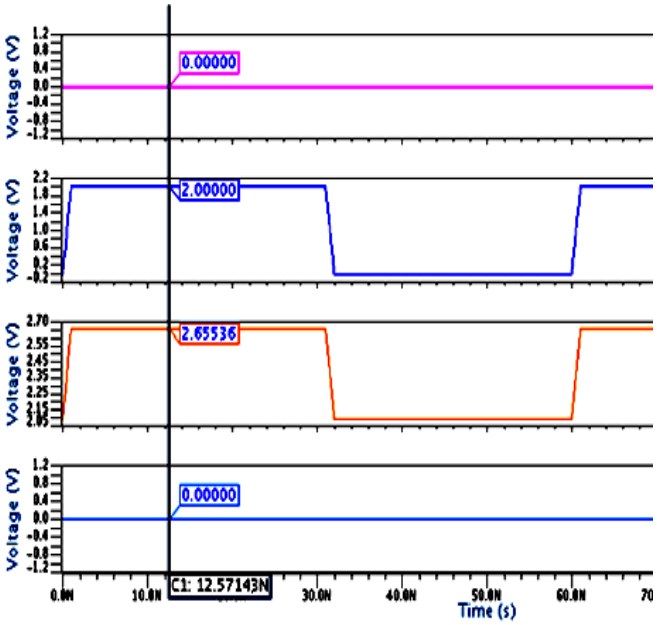

Fig.4 input 010 and output is 0.65V for 3 bit R-2R DAC

And the respective Table I presentation for 3-bit R-2R ladder with technology s 0:35µ is as follow and from the above graph we find that maximum INL for 0:35µ is 0.15.

Table I Integral Non-Linearity

input	ideal o/p	actual o/p	different
000	0.00	0.00	0.00
001	0.25	0.35	0.10
010	0.50	0.65	0.15

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011	0.75	0.85	0.10
100	1.00	1.15	0.05
101	1.25	1.30	0.05
110	1.50	1.60	0.10
111	1.75	1.83	0.08

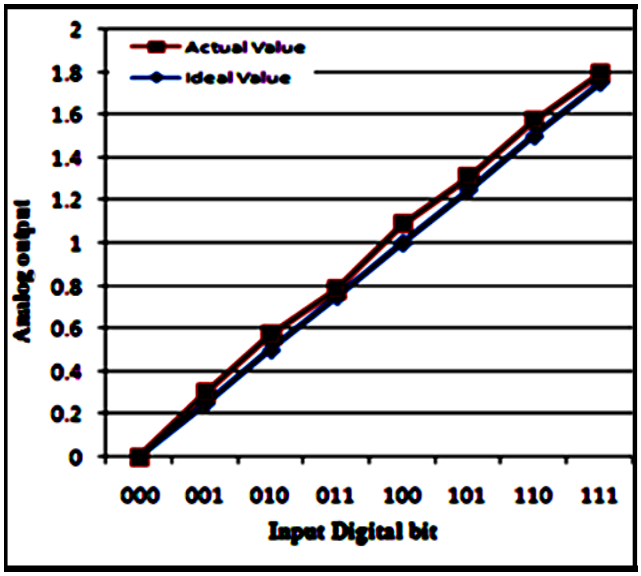

Fig.5: INL for 3 bit R-2R DAC

B. Differential Non-Linearity

DNL = Actual increment height of transition n - Ideal increment height

$$|DNL|_{\max} = \Delta_{IK}(1-\frac{1}{2^n})$$

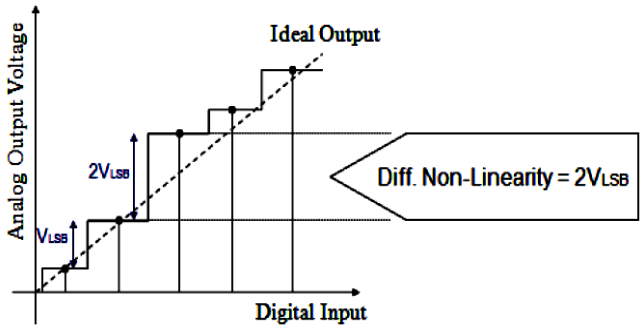

Fig.7:DNL Presentation

Here for 3 bit R-2R DAC input bits are from 000 to 111. And Y axis of fig.7 shows ideal and actual DNL. And the respective Table II presentation for 3-bit R-2R ladder with technology s 0:35µ is as follow and from the above graph we find that maximum DNL for 0:35µ is 0.15

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Table II
Differential Non-Linearity

input	ideal o/p	actual o/p	different
000	0.00	0.00	0.00
001	0.25	0.35	0.10
010	0.50	0.65	0.15
011	0.75	0.85	0.08
100	1.00	1.15	0.15
101	1.25	1.30	0.05
110	1.50	1.60	0.10
111	1.75	1.83	0.08

Highest DNL is resulted at the time of bit changes of 011 to 100.

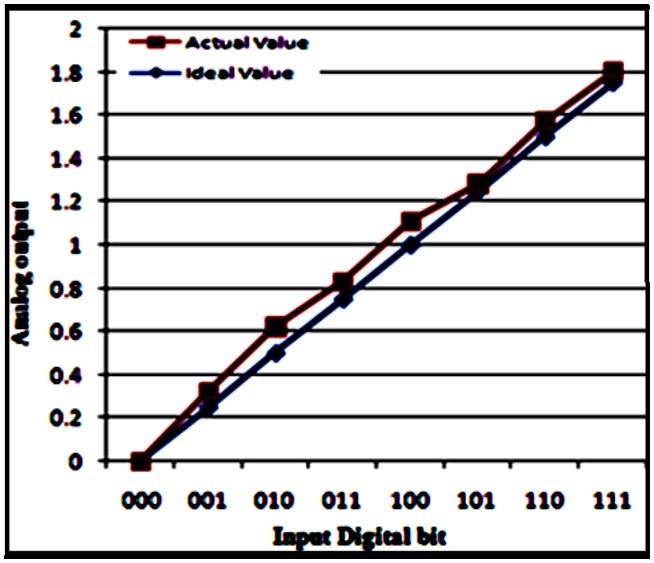

Fig.7: DNL for 3 bit R-2R DAC

V. CONCLUSION

In this paper 3-bit R-2R DAC simulated in 0.35um technology. Power supply of the architecture is 2.2V.maximum INL and DNL is 0.15. and power dissipation is $3.35X10^{-11}$ W. In my simulation result,INL,DNL and power dissipation is very excellent result.

VI. ACKNOWLEDGMENT

Author thanks the team of Laljibhai Chaturbhai Institute of Technology College for the facilities provided and consistent encouragement.

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