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New Delay and Power Analysis for a CMOS Inverter Driving RLC Interconnect

Sohini Mondal, Bishnu Prasad De

Abstract*— In this era, the on-chip interconnect delay is significantly more dominating than the gate delay. Several approaches have been proposed to capture the interconnect delay accurately and efficiently. Here delay and power analysis for a CMOS inverter driving a resistive-inductive-capacitive load is presented. A closed form delay and power model of a CMOS inverter driving a resistive-inductive-capacitive load is discussed. The model is derived from Sakurai's alpha-power law and exhibits good accuracy. The model can be used for the design and analysis of the CMOS inverters that drive a large interconnect RLC load when considering both speed and power. Closed form expressions are also presented for the propagation delay and transition time which exhibit less than 15% error compared to the SPICE for a wide range of RLC loads. Explicit methods are also provided for modeling the short-circuit power dissipation of a CMOS inverter driving a RLC line. The average error is within 22% compared to SPICE for most practical loads.

***Index Terms*—Electronics, CMOS, Delay , Power, RLC Interconnect, SPICE,VLSI (Very large scale integration)**

I. INTRODUCTION

As the minimum feature size for integrated circuits is scaled downwards, the resistive component of the interconnect load become comparable to the gate output impedance and a single lumped capacitor is no longer a valid gate load model. With the decrease of the die size of CMOS integrated circuits, interconnections have become increasingly significant [1]. **If the length of the interconnections increases linearly then the delay will increase quadratically due to the linear increase in both interconnect resistance and capacitance [2]**.Several methods have been introduced to reduce interconnect delay Previously a simple yet realistic MOS model, namely the alpha power law MOS model [14] was introduced to include the carrier velocity saturation effect, which becomes eminent in short channel MOSFETs. The model is an extension of Shockley's square-law MOS model in the saturation region. Since the model is simple, it can be applied for handling MOSFET circuits analytically and can predict the circuit behavior in the sub micrometer region. Using this model, closed form expressions are derived for the delay, the short circuit power and the transition voltage of CMOS inverters.

The Elmore delay model [5] gives the formula to calculate the delay at a specific node by using a formula upon any given RC tree network consisting of several branches. A model expression for CMOS inverter driving capacitive load was first introduced by Burns and Hedenstierna and Jeppson. Large interconnect loads not only affects the performance but also cause excessive power dissipation. A large load degrades the shape of output waveform.

Now a days, with the introduction of portable computers power has become an important factor in the circuit design process. Thus power consumption must be accurately estimated for improving circuit speed when driving long interconnections. Therefore, the circuit level models describing both dynamic power and recently short circuit power have become increasingly important. With the increase in the frequency of operation and the wire sizes, the inductance play an important role in determining the performance of on-chip interconnects.[8-11] During the analysis on-chip interconnects are taken as distributed RLC segments. For this purpose power expressions associated with alpha power law are used to estimate the propagation delay and rise and fall times of a CMOS inverter. Using T-Spice a CMOS inverter propagation delay has been calculated for various values of R, L, C. The transition time is also calculated for various R,L,C values. The short circuit power of the non-step input driving CMOS inverter has also been calculated.

This paper is presented as follows; II. Various mosfet Models, III. Delay Model of a CMOS Inverter Driving RLC load, IV. Power Estimation Techniques, V. **S**imulation Results VI. Conclusion, VII. Acknowledgement, VIII. References IX. About the authors.

II. VARIOUS MOSFET MODELS

A simple and accurate set of equations is required to describe MOSFET characteristics for VLSI circuit design is called the Compact MOSFET Model, and can only be obtained by adopting suitable approximations and appropriate empirical fittings of parameters. The model, with the help of the mathematical equations represents the physical meaning of parameters and is expected to work efficiently. There are three main types of existing compact MOSFET models:-Physical Models: Models which is based on the device physics. Empirical Models: A model which relies on just curve fitting. Table Models: These models are typically in the form of the table.

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Alpha-power law MOSFET Model: [1990]: This model includes the carrier velocity saturation effect, and matches with the SPICE MOS LEVEL3 model. Using this model, closed form expressions are derived for the delay, the short circuit power, and the transition voltage of CMOS inverters. The resultant delay expression input waveform slope effects parasitic drain/source resistance effects and can be used in simulation and/or optimization CAD tools.

A Physical Alpha-Power Law MOSFET Model:[1990]: This model includes: Extension into the sub threshold region of operation. The effects of vertical and lateral high field mobility degradation and Velocity saturation. Threshold Voltage roll off. This model is verified by HSPICE simulations and measured data[3]. **EKV Model:[1995]:**This model includes mobility reduction, velocity saturation, channel length modulation, short channel and narrow channel effects. This model has only 9 physical parameters, 3 fine tuning fitting coefficients, 2 additional temperature parameters. In this model, thermal noise power spectral density is related with the total charge in the channel [2].

Modified Sakurai-Newton Current Model:[2003]: This model was proposed by Makaram M. Mansour, Mohammad M. Mansour and Amit Mehrotra. This model takes into account the dependence of carrier velocity on the vertical field, carrier velocity saturation, and dependence of the drain current on the transistor gate width. The MSN-model matches HSPICE level 49 simulations to CMOS technologies over a wide range of transistor widths, fan outs and input rise/fall times [4]. **Extended –Sakurai-Newton MOSFET Model:[2009]:**It is an extension of the nth power law model. The ESN model is further used to improve the Elmore Delay prediction of CMOS inverter operated at low supply voltages.

An accurate analytical I-V model for sub-90-nm MOSFET:[2011]: The accuracy of this model is verified by comparing its results with those of HSPICE for the 90, 45, 65 and 32 nm CMOS technologies. The model shows better accuracy than the nth power law model. The validity of the model is also verified in the presence of process variations and negative bias temperature instability. This model can accurately predict the minimum supply the voltage required for the target yield.

Some of the existing MOSFET Delay Models are: **the Elmore Delay Model:** the Elmore delay is defined as the centroid of the impulse response h(t) of the system. By the Elmore delay model the propagation delay of a CMOS gate can be approximately estimated by converting it into an equivalent inverter. The size of the PMOS and NMOS used in the equivalent inverter represent the effective strengths of the actual pull-up and pull-down paths respectively. In order to derive analytical delay expressions for CMOS gates in the UDSM region, a realistic yet simple MOS model is required.

The Alpha-Power Law Inverter Delay Model:

$$\tau di = \sum_{j=1}^{N} Cj \sum_{for\ all\ k \in Pij} Rk$$

In the Alpha-power law Inverter Delay model the modified centroid can accurately predict the delay values for wide range of supply voltage. For supply voltage variation less than 3Vth the modified centroid of power based delay metric can be used. **Nth Power law Inverter Delay Model:** Nth Power Law Inverter Delay model is sometime better than circuit simulations, as this gives insight into delay dependence on parameters. Elmore delay model calculation is done by considering the general RC tree network as shown in fig.1, the following path definitions can be made-Let P_i denote the unique path from the input node to the node, i=1,2,3,4…….N..Let $P_{ij} = P_i \cap P_j$ denote the portion of the path between the input and the node I, which is common to the path between the input and node j. Assuming input signal is a step impulse at time t=0, the ELMORE DELAY at node i can be calculated as,

III. DELAY MODEL OF A CMOS INVERTER DRIVING RLC LOAD

An analytical expression describing the behavior of a CMOS inverter driving a lumped RLC load based on Sakurai's alpha-power law model [11] is presented. The corresponding circuit schematic is given in Figure 1.

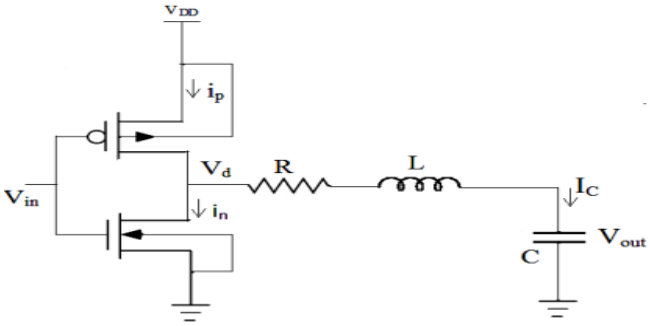

Figure 1. A CMOS Inverter Driving a RLC load

The simple yet realistic alpha-power law model, which is an extension of the Shockley's square law MOS model in the saturation region accurately, describes the effects of short-channel behavior, such as velocity saturation, while providing a tractable solution. To characterize the –I-V behavior of the ON transistor the linear region of alpha power model has been considered as a large portion of the circuit operation occurs within this region under the assumption of a step or a fast ramp input signal. .When the input to the inverter is a unit step or a fast ramp, Vout is initially larger than (V_{GS}-V_T) for a short period of time than for the case of a slow ramp. Therefore, the circuit operates in linear region for a greater portion of the total transition time for a large RLC interconnect load. When the load resistance is large, a large IR voltage drop occurs across the load resistor once the capacitor begins to discharge, thus V_{DS} is nearly immediately less than (V_{GS}-V_T). The N-channel device operates in the linear region once the step input goes high. However, if the input waveform increases more slowly or the load impedance is small, the inverter operates in saturation region for longer time period before switching to the linear region. Only the falling output (rising input) waveform has been considered in this paper. The following analysis, however, is equally applicable to a rising output (falling input) waveform. The lumped load is modeled as a resistor in series with an inductor and a capacitor. The current through the output load capacitance is of same magnitude and of opposite polarity to that of the N-channel drain current (the P-channel current is ignored under the assumption of the step or fast ramp input). The Capacitive Current is,

$$i_c = C\frac{dV_{out}}{dt} = -i_d \qquad (1)$$

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Where, C is the output capacitance, vout is the voltage across the capacitance C,ic is the current discharged from the capacitor, and id is the drain current through the N-channel device.

According to the alpha power law, the N-channel linear drain current is given by [11],

$$-C\frac{dV_{out}}{dt}=\frac{I_{d0}}{V_{do}}\left(\frac{V_{GS}-V_T}{V_{DD}-V_T}\right)^{\alpha}V_{DS};\forall V_{GS}\geq V_T, V_{DS}\leq V_{GS}-V_T \quad (2)$$

I_{d0} represents the driver current of the MOS device and is proportional to W/L, V_{d0} represents the drain to source voltage at which velocity saturation occurs with $V_{GS}=V_{DD}$, and is a process dependent constant and α models the degree by which velocity saturation affects the drain to source current, $1\leq\alpha\leq 2$ where α=1 corresponds to a device operating strongly under velocity saturation ,while α=2 represents a device with negligible velocity saturation.V_{DD} is the supply voltage, and V_T is the MOS threshold voltage (where V_{TN} (V_{TP}) is the N-channel (P-channel) threshold voltage).

Assuming a unit step input is applied to the circuit shown in Figure 1, can be derived from (2). The linear equation, written in Laplace Transform form is-

$$-CsV_{out}(s)+CV_{out}(0)=\mu_{d0}V_{out}(s)+\mu_{d0}RI_c(s)+\mu_{d0}LsI_c(s)$$
$$or, s^2\mu_{d0}LCV_{out}(s)+s\mu_{d0}RCV_{out}(s)+sCV_{out}(s)+\mu_{d0}V_{out}(s)$$
$$=s\mu_{d0}LCV_{out}(0)+\mu_{d0}RCV_{out}(0)+CV_{out}(0) \quad (3)$$

Where, $\mu_{d0}=\frac{I_{d0}}{V_{d0}}$ is the saturation conductance.

Equation (3) yields,

$$V_{out}(t)=V_{out}(0)\left(\varsigma_1 e^{-\xi_1 t}+\varsigma_2 e^{-\xi_2 t}\right)$$

Where, $\xi_{1,2}=\frac{-\gamma\pm\sqrt{\left(\gamma^2-\frac{4}{LC}\right)}}{2}, \gamma=\frac{\mu_{d0}R+1}{\mu_{d0}L}$,

$$\varsigma_1=\frac{\gamma-\xi_1}{\xi_2-\xi_1} and \varsigma_2=\frac{\gamma-\xi_2}{\xi_1-\xi_2} \quad (4)$$

From (4), the propagation delay of a CMOS inverter can be calculated as,

$$t=\frac{\ln(\varsigma_2)+\ln\left(\frac{V_{out}(0)}{V_{out}(t)}\right)}{2\xi_1+\xi_2} \quad (5)$$

For 50% delay,

$$t_{PD}=\frac{\ln(\varsigma_2)+0.693}{2\xi_1+\xi_2} \quad (6)$$

The transition time of a CMOS inverter driving a lumped RLC load calculated at the 90% point is, t_{tr} is,

$$t_{tr}=\frac{\ln(\varsigma_2)+2.3}{2\xi_1+\xi_2} \quad (7)$$

Additional delay expressions that are used for determining short circuit power are,

$$t_{V_{TN}}=\frac{\ln(\varsigma_2)+\ln\left(\frac{V_{TN}}{V_{DD}}\right)}{2\xi_1+\xi_2} \quad (8)$$

$$t_{V_{TP}}=\frac{\ln(\varsigma_2)+\ln\left(\frac{V_{DD}+V_{TP}}{V_{DD}}\right)}{2\xi_1+\xi_2} \quad (9)$$

Equations (8) and (9) describe the time for the output voltage to change by a threshold voltage from either ground or V_{DD} for an N-channel or P-channel device, respectively.

IV. POWER ESTIMATION TECHNIQUES

Power consumption has become one of the premier issues in VLSI circuit design. There are two primary contributions to the total transient power dissipated by a CMOS inverter, dynamic power and short-circuit power dissipation [8-11], [14- 15]. The short-circuit power is often neglected, and the dynamic power is assumed to be dominant. Dynamic power is the energy required to charge and discharge a load capacitance C and is characterized by, CV^2f ; where V is the source voltage and *f* is the switching frequency. The dynamic power is independent of the load resistance.

This project report analyses a closed form expression for modeling the short circuit power in a CMOS inverter driving RLC interconnects. The logic stage following a large RLC load may dissipate significant amount of short-circuit power due to the degraded waveform originating from the CMOS inverter driving a RLC load (Figure 2). In the region where the input signal is switching between V_{TN} and (V_{DD}+V_{TP}), a DC current path exists between V_{DD} and ground. The excess current dissipated during this region is called the short-circuit current [14]. Short-circuit current occurs due to a slow input transition, and for a balanced inverter, the peak current occurs near the middle of the input transition.

The total short-circuit current I_{SC} can be estimated by approximated ISC as a triangle. Therefore, the integral of ISC is the area of a triangle, ½ X (base X height) In terms of the short-circuit current, the height can be modeled as I_{peak} and the base can be modeled as t_{base}. *I peak* is the maximum saturation current of the load transistor and depends on both V_{GS} and V_{DS}, therefore, *I peak* is both input waveform and load dependent. t_{base} is the time during which both N-channel and P-channel transistors are turned on, permitting a DC current path to exist between V_{DD} and ground. This time occurs over the region, $V_{TN}\leq Vin\leq V_{DD}+V_{TP}$. Therefore, t_{base} is found from the difference between (8) and (9), $|(V_{TP}-V_{TN})|$.

The total short-circuit current multiplied by *f* and V_{dd} is the short-circuit power. The short-circuit power. The short-circuit power dissipation Psc of the following stage for one transition (either rising or falling edge) can, therefore, be approximated by,

$$P_{SC}=\frac{1}{2}base\times height V_{DD}f \quad (10)$$

Subtracting (8) from (9) forms the logarithmic quotient,

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$$t_{base} = \left| \ln\left(\frac{V_{TN}}{V_{DD} + V_{TP}} \right) \right| \frac{1}{2\xi_1 + \xi_2} \quad (11)$$

By inserting this expression t_{base} for into (10), the short-circuit power dissipation P_{sc} of a CMOS inverter following a lumped RLC load over both the rising and falling transitions can be calculated as,

$$P_{SC} = \left| \ln\left(\frac{V_{TN}}{V_{DD} + V_{TP}} \right) \right| \frac{1}{2\xi_1 + \xi_2} I_{peak} f V_{DD} \quad (12)$$

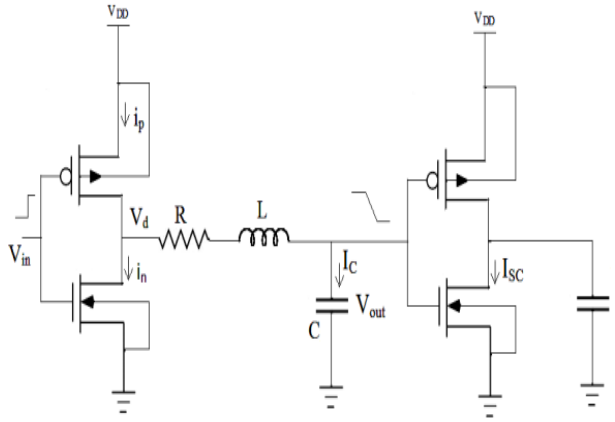

Figure2. Non-Step Input Driving CMOS Inverter Stage Creates Short Circuit Power

V. SIMULATION RESULTS

The accuracy of the analytic delay model as compared to the SPICE is tabulated in table 1 to 6.Table 1 represents the estimation of propagation delay (t_{pd}) of an inverter driving RLC Load For L=1nh.The average error of the propagation delay t_{pd}, as compared with SPICE is 12.02%. Table 2 represents estimation of propagation delay (t_{pd}) of an inverter driving RLC load for c=1pF.The average error of the propagation delay t_{pd} ,when c=1pF as compared with SPICE is 18.56%. Table 3 gives the estimation of transition time (t_{tr})of an inverter driving RLC load for L=1nH and the average error is 17.98%. Table 4 gives the estimation of transition time (t_{tr}) of an inverter driving RLC load for c=1pf. Equations (6) and (7) can be used to estimate the propagation delay and transition time of a CMOS inverter driving a RLC interconnects line. Since the shape of the output waveform is now known, (8) and (9) can also be used with (7) to estimate the short-circuit power dissipation of a CMOS gate loading the high impendence interconnect line. The short-circuit power derived from (11) for a wide variety of RLC loads between the CMOS inverter stages as shown in Figure 2 is compared with SPICE and given in Table 5 and 6. Table 5 shows the short circuit power dissipated by inverter circuit for various R and C values for constant L. The result is compared with SPICE and the average error is 17.7%. Table 6 presents short circuit power dissipated by inverter circuit for various R and L values for C=1fF. The result is compared with SPICE value and average error is 19.48%.

Table 1: Estimation Of Propagation Delay (tpd) Of An Inverter Driving RLC Load For L=1nh

R(ohm)	L(n H)	C(Pf)	t_{PD} (p s) (SPICE)	t_{PD} (p s) (Proposed Method)	%Error
10	1	0.01	32.765	41.46	20.12
10	1	0.05	121	123.45	7.98
10	1	0.1	167.98	178.67	8.23
100	1	0.01	41.67	44.99	3.89
100	1	0.05	120.56	126.34	17.31
100	1	0.1	158.66	180.98	21.67
1k	1	0.01	43.45	45.9	6.78
1k	1	0.05	98.78	128.7	16.91
1k	1	0.1	133.98	168.082	4.67

Table 2: Estimation of propagation delay (t_{pd}) of an inverter driving RLC load for c=1pF

R(ohm)	L(n H)	C(Pf)	t_{PD} (p s) (SPICE)	t_{PD} (p s) (Proposed Method)	%Error
10	0.5	1	140.167	180.45	22.8
100	0.5	1	141.67	187.3	23.4
1000	0.5	1	147.673	192.8	18.9
10	1	1	123.564	151.89	21.67
100	1	1	148.990	163.89	11.45
1000	1	1	150.662	192.4	12.75
10	10	1	223.67	167.34	14.67
100	10	1	163.993	184.2	17.98
1000	10	1	221.30	251.5	23.43

TABLE 3: Estimation of transition time (t_{tr}) of an inverter driving RLC load for L=1nH

R(ohm)	**L(n H)**	**C(Pf)**	**t_{tr} (p s) (SPICE)**	**t_{tr} (p s) (Proposed Method)**	**% Error**
10	1	0.01	92.004	98.76	5.19
10	1	0.05	194.67	205.67	14.19
10	1	0.1	245.55	278.9	21.89
100	1	0.01	89.90	97.33	6.95
1100	1	0.05	198.89	207.89	18.67
100	1	0.1	276.89	298.56	16.13
1k	1	0.01	82.007	97.89	22.4
1k	1	0.05	198.66	203.56	12.94
1k	1	0.1	245.99	298.65	13.98

TABLE 4: Estimation of transition time (t_{tr}) of an inverter driving RLC load for c=1pf

R(ohm)	**L(n H)**	**C(Pf)**	**t_{PD} (ps) (SPICE)**	**t_{PD} (ps) (Proposed Method)**	**%Error**
10	0.5	1	197.086	248	20.53
10	1	1	239.45	254.6	5.95
10	10	1	213.717	247.1	13.51
100	0.5	1	187.6	241.1	22.21
100	1	1	222.184	242.56	8.34
100	10	1	212.274	246.3	13.78
1k	0.5	1	206.098	236.1	14.87
1k	1	1	198.926	228.1	12.79
1k	10	1	185.98	208.4	16.9

TABLE 5 : Estimation of short circuit power(P_{sc}) for l=0.5nh,vdd=1.8v,f=0.2GHz

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R(ohm)	L(nH)	C(Pf)	Power(mW) Proposed Method	Power(mW) Spice	% Error
10	0.5	0.3	23.085	18.389	20.61
10	0.5	0.5	26.315	22.980	14.15
10	0.5	1	31.165	24.456	16.51
100	0.5	0.3	25.987	21.810	19.71
100	0.5	0.5	26.932	22.678	17.59
100	0.5	1	30.458	25.997	17.71
1000	0.5	0.3	26.528	20.567	21.61
1000	0.5	0.5	29.387	23.67	20.31
1000	0.5	1	33.786	29.174	18.61

TABLE 6: Estimation of short circuit power (Psc) for c=1fF, vdd=1.8v,f=0.2GHz

R(ohm)	**L(nH)**	**C(fF)**	**Power (mW) Proposed Method**	**Power(mW) Spice**	**%Error**
10	10	1	25.567	22.345	12.765
100	10	1	26.769	24.897	18.942
1000	10	1	25.887	20.145	21.870
10	40	1	26.774	20.171	21.023
100	40	1	27.773	20.135	25.568
1000	40	1	67.889	60.670	17.347
10	80	1	23.987	20.478	22.45
100	80	1	25.67	21.551	17.89
1000	80	1	66.78	60.339	17.554

V. CONCLUSION

A simple yet accurate expression for the output voltage of a CMOS inverter driving RLC load is analyzed in this paper. With this expression, equations characterizing the propagation delay and transition time of a CMOS inverter driving RLC load are presented. This estimated transition time is compared with SPICE result for various R, L and C. For different R, C and constant L the average error is 17.98% and for various R, L and constant C, the average error is 11.38%. Similarly the propagation delays of CMOS inverter driving various RLC loads are estimated and are compared with SPICE. For various R, C and constant L, the average error is 12.02% and for various R, L and constant C, the average error is 18.56%. Therefore, due to the simplicity and accuracy of these expressions, the delay and power characteristics of a CMOS inverter driving high impedance RLC interconnect line can be efficiently estimated.

VI. ACKNOWLEDGEMENT

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