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Design of A Low Voltage Low Power CMOS Current Mirror with Enhanced Dynamic Range

Ramanand Harijan, Padma Devi, Pawan Kumar

Abstract*— A novel cascode current mirror (CM), suitable for operation at low voltage levels is presented. The mirror has high input and high output voltage swings. The presented current mirror circuit combines the advantages of wide input swing, wide output swing and large output resistance capability which makes it attractive for low-voltage and low power application. Based on IBM 0.18um MOS model parameters, TSPICE simulation results show that the input current range of 1uA to 2mA with 882.83MHz bandwidth for the presented level shifted low voltage current mirror circuit. The power dissipation has improved by more than 40%.

Index Terms*— Current mirror, *Low voltage current mirror, level shifted Current mirror, Level shifted low voltage current mirror, Dynamic range.

I. INTRODUCTION

Now days the portable electronics has made low power circuit design extremely desirable. All efforts eventually converge on decreasing the power consumption entailed by ever shrinking size of the circuits enabling the portable gadgets. Reducing power supply voltage is a straightforward method to achieve low power consumption. The low power and low voltage CMOS techniques were applied extensively in analog and mixed mode circuits for the compatibility with the present IC technologies. Designing high – performance analog circuits is becoming increasingly challenging with the persistent trend towards reduced supply voltages. The current mirror (CM) is one of the most basic building blocks both in analog and mixed mode VLSI circuits especially for active elements like op-amps, current conveyors, current feedback amplifiers etc[2],[5],[6]. At large supply voltages, there is a trade – off among speed, power and gain. The main characteristics under consideration are power, voltage, dynamic range, bandwidth, low offset voltage, high output voltage swing. The use of current mirrors with low input voltage is especially important for implementation of VLSI test circuits which employ current sensing techniques [5].The desire for portability of electronic equipment generated a need for low power systems in battery operated products like hearing aids, implantable cardiac pacemakers, cell phones, and hand held multimedia terminals. Low power dissipation is attractive, and perhaps even essential in these applications to have reasonable battery life and weight. The ultimate goal in design is close to having battery- less systems, because the battery contributes greatly to volume and weight.[1],[3],[4].

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II. LOW VOLTAGE CURRENT MIRROR

One of the most fundamental building blocks of analog integrated circuit is the Low Voltage current mirror .Current mirror is enable a single current source to supply mirrors are output impedance and voltage headroom. The output impedance determines the variation of the mirrored current when the applied voltage varies. Higher output impedance implies less current variation with applied voltage and hence a more stable current source Voltage headroom specifies how much voltage drop across the current mirror is required ton operate the current mirror reliably. This is especially important for low voltage circuit design [2].

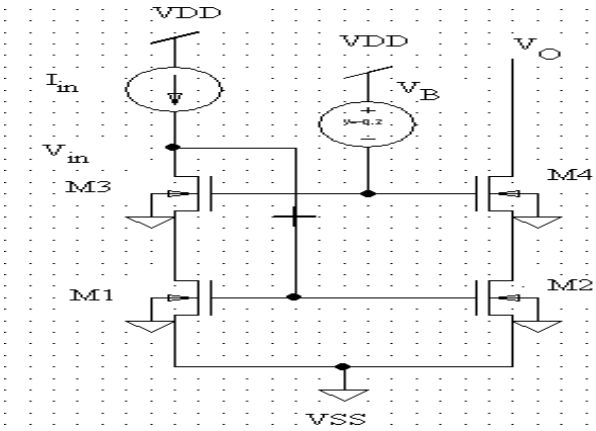

Figure 1: Low Voltage Current Mirror

The low voltage cascode current mirror shown in Figure 1 .We assumes that the current mirror transistors M1 and M2 have identical, aspect ratio. $A_M = \frac{W_1}{L_1} = \frac{W_2}{L_2}$ Where W_1 and W_2 are the transistor channel width and L_1 and L_2 are the transistor length. Similarly the transistor M3 and M4 are assumed the same aspect ratio $A_C = \frac{W_3}{L_3} = \frac{W_4}{L_4}$ .The aspect ratio A_M may be different from the aspect ratio A_C [3],[5]. In the analysis of the dynamic range the same aspect ratio of A_M and A_C and we use standard Schman –Hodges transistor model for the transistor in the saturation region and we neglected the bulk effect and assume that all the NMOS transistors have the identical. Low voltage current mirror input current I_{in} we find the gate- source voltages and drain -source voltages [3]

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$$V_{GS1} = V_{tn} + \sqrt{\frac{2I_{in}}{KA_M}} \quad (1)$$

Gate to source voltage of transistor M3

$$V_{GS3} = V_{tn} + \sqrt{\frac{2I_{in}}{KA_C}} \quad (2)$$

Drain to source voltage of transistor M1 is

$$V_{DS1} = V_{BC} - V_{tn} - \sqrt{\frac{2I_{in}}{KA_C}} \quad (3)$$

Drain to source voltage of transistor M3 is

$$V_{DS3} = V_{GS1} - V_{DS1}$$

$$= 2V_{tn} - V_{BC} + \sqrt{\frac{2I_{in}}{K}}\frac{1}{\sqrt{A_M}} + \frac{1}{\sqrt{A_C}} \quad (4)$$

Where, V_{tn} is the transistor threshold voltage, V_{BC} is the bias or gate voltage of transistor M3 and M4 and K is the transconductance parameter. Requiring $V_{GS} - V_{tn} \leq V_{DS}$ for both M1 and M3 result in:

$$\sqrt{\frac{2I_{in}}{K}}\left(\frac{1}{\sqrt{A_M}} + \frac{1}{\sqrt{A_C}}\right) + V_{tn} \leq V_B \quad (5)$$

Biasing voltage

$$V_B \leq 2V_{tn} + \sqrt{\frac{2I_{in}}{K A_M}} \quad (6)$$

In Figure 1 low voltage current mirror, biasing voltage V_B is fixed when I_{in} increases, voltage of the gate –source voltage V_{GS3} of transistor M3 and V_{in} will increase, and voltage level at the drain terminal of M1 decrease. There by M1 enter the triode region which determine the upper limit of I_{in}.below equation (7) ensure the saturation of M1 and determine the maximum value of I_{in} for given value of the cascade bias voltage V_B we find

$$I_{in,max} = \frac{K}{2} A_M (V_B - V_{tn})^2 \left(\frac{\sqrt{A_C/A_M}}{1+\sqrt{A_C/A_M}}\right)^2 \quad (7)$$

Equations(7) ensure the saturation of M3 and determine the minimum value of I_{in} we find

$$I_{in,min} = \frac{K}{2}(V_B - 2V_{tn})^2 A_M \quad (8)$$

Maximum value of the bias voltage even at the minimum value of input current equation (8) determine, and equation (8) determined the value of A_C and A_M which determined the saturation of M1 and the maximum value of input current . To ensure Saturation operation of transistors M1 and M3 the input current range determined by

$$\frac{K}{2} A_M (V_B - 2V_{tn})^2 \leq I_{in} \leq \frac{K}{2} A_M (V_B - V_{tn})^2 \left(\frac{\sqrt{A_C/A_M}}{1+\sqrt{A_C/A_M}}\right)^2 \quad (9)$$

In a practical design procedure equation(8) can be used to determine the maximum value of the bias voltage which will ensure saturation of M3 even at the minimum value of input current, and equation (6) can then be used to determine values of A_C and A_M which will ensure saturation of M1, even at the maximum value of input current. In the important special case of $I_{in,minimu} = 0$ we find from (8) $V_B \leq 2V_{tn}$. From equation (7) we then find the following design constraint on A_C and A_M

$$A_M \left(\frac{\sqrt{A_C/A_M}}{1+\sqrt{A_C/A_M}}\right)^2 \geq \frac{2I_{in,max}}{V_T^2 K} \quad (10)$$

Assuming as a typical case W1 = W3 and L1 = L3 i.e. identical aspect ratios for the mirror transistors and the cascode transistors, we find

$$A_M = A_C = \frac{W}{L} \geq \frac{2I_{in,max}}{V_T^2 K} \quad (11)$$

In this case the effective gate-source voltage of the mirror transistors M1 and M2 is

$$V_{GS1} - V_{tn} = \sqrt{\frac{2I_{in}}{KA_M}} = \frac{V_{tn}}{2}\sqrt{\frac{I_{in}}{I_{in,max}}} \quad (12)$$

In this case the minimum output voltage of the current mirror is and is independent of the input current.

$$V_{out,min} = V_B - V_{tn} = V_{tn} \quad (13)$$

In a high precision current mirror one would like to have as large an effective gate-source voltage as possible in order to minimize the effect of threshold voltage mismatch. It is evident that the effective gate-source voltage $V_{GS1} - V_{tn}$ can be increased above the value given by equation(15) if A_C is increased, i.e. a larger aspect ratio is used for the cascade transistor. In this case the cascode transistor requires a smaller effective gate-source voltage for a given value of input current, leaving more headroom for the drain-source voltage of the mirror transistor. Introducing $N = A_C/A_M$ we find

$$A_M = \left(\frac{1+N}{N}\right)^2 \frac{2I_{in,max}}{(V_B - V_{tn})^2 K} \quad (14)$$

And

$$V_{GS1} - V_{tn} = \frac{N}{1+N}(V_B - V_{tn})\sqrt{\frac{I_{in}}{I_{in,max}}} \quad (15)$$

The small signal output resistance of the mirror is given by

$$r_{out} = \frac{1}{g_{ds2}}\left(1 + \frac{g_{dm4}}{g_{ds4}}\right) \approx \frac{1}{g_{ds2}}\frac{g_{m4}}{g_{ds4}} \quad (16)$$

As g_{m4}/g_{ds4} is inversely proportional to the square root of A_C we find that the output resistance is inversely proportional to N. Thus, the higher effective gate-source voltage of the mirror transistors is achieved at the expense of a reduced output resistance..

III. LEVEL SHIFTED CURRENT MIRROR

Shown in figure 2 level shifted current mirror, the simple current mirror topology [10] requires input voltage (V_{in}) at least one V_{tn} and unsuitable for low voltage application. Level shifted current mirror operates at low voltage with the advantage of low input output voltage requirement, incorporates a level shifter PMOS transistor M5 (biased through a current I_{bias1}) at input port. For this structure, we have

$$V_{DS1} = V_{GS1} - V_{GS5} \quad (17)$$

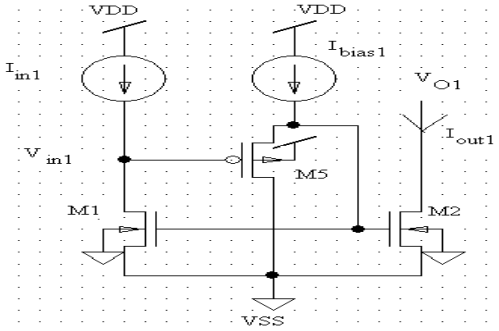

Figure 2: Level Shifted Current Mirror

Where V_{DS1} drain to source and V_{GS1} gate to source voltage of M1, V_{GS5} is the gate to source voltage of M5. A level shifted current mirror circuit structure is shown in Figure 2 M3 is used to shift the voltage level at the drain terminal of M1.

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V_{in} is a characteristics parameter of a low voltage current mirror and decides the range of input voltage swing in such circuits. The bias current (I_{bias1}) decide the operation region of M1. For example, low value of I_{bias1} forces M3 to operate in sub threshold region, I_{bias1} high I_{bias1} ensures M5 operates the triode region. For high value V_{DS2}, M2 operates in saturation region. Gate voltage of M1 is high correspondingly input current is also high. Thus V_{in} can be calculated for this circuit structure if we know the values of V_{GS1} and V_{GS5} since $V_{tp} > V_{tp}$, there is a difficulty to keep the condition $V_{GS1} - V_{GS5} > 0$ valid in a level shifter based circuit over a wide range of I_{in1}. One of the solutions is to use a lateral p-n-p transistor for level shifting, and now $V_{in1} - V_{GS1} - V_B > 0$ approximates as 0.7V and V_{GS1} is always more than 0.8v (if we assume V_{tn}=0.8v). As the device sizes are reducing and V_t is also reducing and there will be a situation where $V_{GS1} - V_B > 0$ will not be valid and hence we may not be able to use p-n-p transistor. Thus, there is a need to have an alternative a p-n-p transistor and the use of a PMOS transistor is the most obvious choice..

IV. LOW VOLTAGE LEVEL SHIFTED CURRENT MIRROR

Figure 3 shown the level shifted low voltage cascode current mirror it is the combination of low voltage and level shifted current mirror and The combined the low voltage and level shifted current mirror present a level shifted low voltage current mirror. In this topology to achieve larger dynamic range for low voltage operation. The operation of M5 and M3 are similar in the Figure 2 of M 5 and M1 we adopt the same assumptions in low voltage in this current mirror. We assume figure 3.5 the threshold voltage of M5 is V_{tp} , when the level shifted current mirror transistor M5 and M1 on must be conditions satisfied $V_{GS3} > V_{tn}$ and $V_{GS5} > V_{tp}$, but when $V_{tp} > V_{tn}$ there is a difficulty to the condition satisfy $V_{DS3} > 0$ wide range of input current Iin2.We literature survey we can find the most suitable operation mode of M5 is sub threshold region because here low input current and in saturation region high input current of M1 and M3. The assumption under the $V_{SD5} > 3V_t$,the sub-threshold drain current of transistor M5 can be expressed by

$$I_{bias2} \approx \frac{W_5}{L_5} I_{DO5} \exp\left(\frac{V_{SG5} - |V_{tp}|}{nV_T}\right) \qquad (18)$$

In above equation (18) W5 and L5 represent the channel width and length of transistor M5, and V_T (approximately ≈26mv at room temperature) [2] is thermal voltage. The Constant n and I_{DO5} are process parameters. Typically value of $I_{DO5} \approx 20nA$ and n lie between 1.2 and 2.0 [2]. For the sub-threshold operation of transistor M5 ($V_{SG5} \approx |V_{tp}|$) and saturation operation of transistor M1 and M3, find

$$I_{in2} \leq \frac{kA_C V_{SG5}^2}{2} \leq \frac{kA_C V_{tn}^2}{2} \qquad (19)$$

$$V_{tn} \leq V_{in2} \leq V_{SG5}\sqrt{\frac{A_C}{A_M}} + V_{tn} \leq V_{tn}\left(1 + \sqrt{\frac{A_C}{A_M}}\right) \qquad (20)$$

When transistors M1, M3, M5 are in sub-threshold region, and the gate to source voltage of M1, M3 and M5 are almost near to their threshold voltages, can find

$$I_{in2} \leq \frac{I_{DO1} W_1}{L_1} \qquad (21)$$

$$V_{in2} = nV_T \ln\frac{I_{in2}}{I_{DO1}}\frac{L_1}{W_1} + V_{tn} \leq V_{tn} \qquad (22)$$

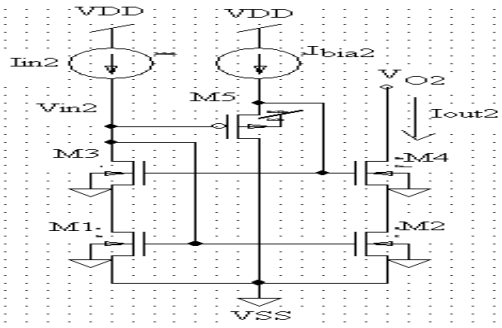

Figure 3: Level Shifted Low Voltage Cascode Current Mirror

Sub threshold operation of transistor M5, when the input current Iin2 increases input voltage Vin2 increases, transistor M5 shifts the voltage level at gate terminal of M3, there for this current mirror improved the upper limit of the input current, compared to low voltage cascode current mirror. The current through M5 should be small enough to keep in transistor M5 in sub-threshold region. Correspondingly channel width and length ratio of transistor M5 should also be large. The current through M1 and M3 should be large to keep it in saturation region. Level shifted low voltage cascode current mirror input current Iin2 is low, transistor M1 and M3 are operate in sub-threshold region. When input current (i.e. Iin2) is low, M3 and M1 will operate in sub-threshold region. If only M5 operates in sub-threshold region and M1-M4 are restricted to operate in saturation region, this CM will possesses better frequency response and the lower limit of the input current is slightly higher. And the minimum output voltage of the level shifted low voltage cascode current mirror is equal to:

$$V_{O2,min} = V_{GS2} + V_{GS4} - 2V_{tn} = \sqrt{\frac{2I_{in}}{K A_M}} + \sqrt{\frac{2I_{in}}{KA_C}} \qquad (23)$$

V. SIMULATION RESULT

The circuit shown in Figure 1 Low voltage current mirror and Figure 3 level shifted low voltage current mirror is simulated using 0.18µm IBM MOS model parameters technology with DC supply voltage of 1V. The biasing voltage V_B in figure 1 and biasing current I_{bias} in figure 3 are -0.2v and 0.3µA respectively. Transistor M1 and M3 ensure the saturation operation biasing voltage (V_B) and Ibias2 selected ensure the operate M5 sub-threshold region gate to source voltage M5 is slight lower than V_{tn}. Table 1 summarizes the (*W/L*) ratios of MOSFETs used in circuits. The input characteristics of LVCM is shown in figure 4 and current transfer characteristics shown in figure 5 and the input characteristics of LSLVCM is shown in Figure 6 and current transfer characteristics shown in Figure 7.it can be observed that the presented level shifted low voltage cascode current mirror improved dynamic range. The frequency response of level shifted low voltage Cascode current mirror is shown in figure 8. The frequency response of LSLVCM is dependent on the capacitive load (Cload). In Figure 8 the -3db banwidth is 887.83Mhz for a load capacitance of 50 pF.Power dissipation result of LSLVCM supply voltage 1 volt and I_{in} of 1mA.

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Width and length of transistors (M3 & M4 and M1 & M2) are kept same. Transient analysis is used to calculate the power dissipation in the current mirror. Figure 9 shows power dissipation results. Power results are reported at the end of transient simulation in the output file.

A. Width and Length Used In Low Volatge, Level Shifted, Low Voltage Level Shifted Current Mirror

Table I. W/L of transistors used in current mirrors

MOSFETS	Type	Width	Length
M1,M2,M3,M4	NMOS	20 µm	0.5 µm
M5	PMOS	10 µm	0.3 µm

B. Comparison of Various parameters With Reference Work[5]

Table II. Comparison of various parameters with reference work [5]

Property	Reference Work [5]	Present Work
Dynamic Range	1µA to1mA	1µA to 2mA
Supply voltage	1volt	1volt
Bandwidth	723MHz	882.83
Power	-	100 µW

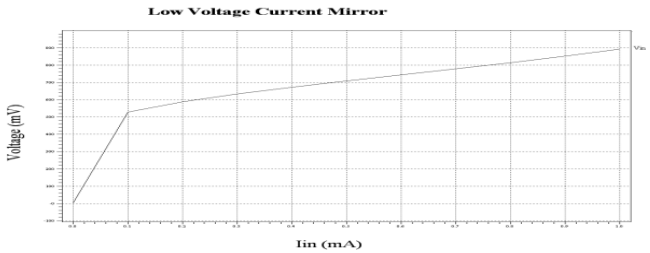

Figure 4: Input characteristics LVCM

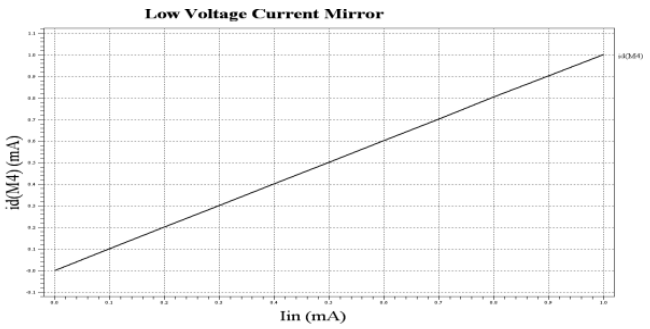

Figure 5: Current transfer characteristics LVCM

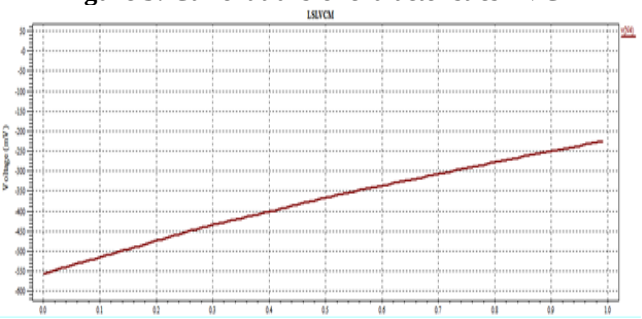

Figure 6: Input characteristics of LSLVCM

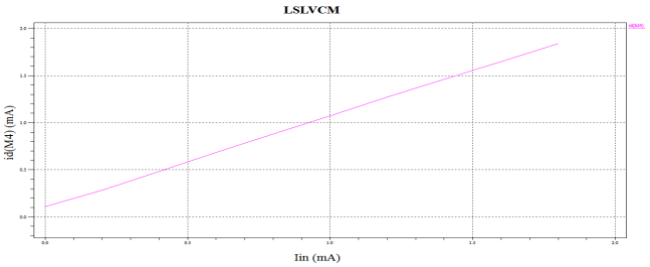

Figure 7: Current transfer characteristics of LSLVCM

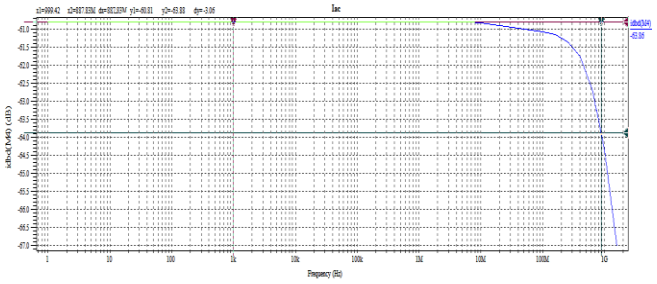

Figure 8: Frequency response of LSLVCM

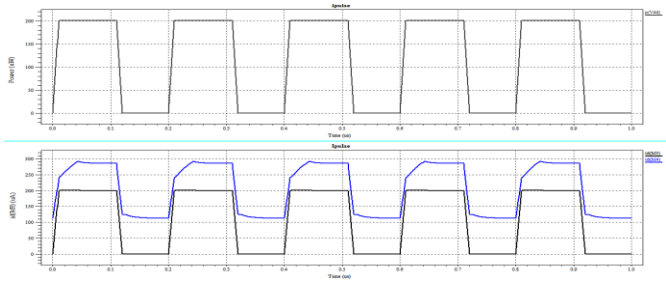

Figure 9: Power dissipation of LSLVCM

C . Comparison Of Dynamic Range Low Voltage Current Mirror and Level Shifted Low Voltage Current Mirror

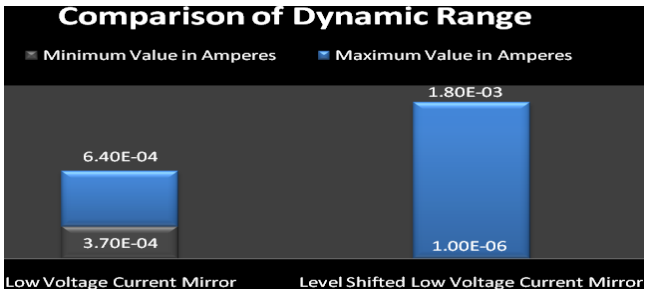

Figure 10: Low voltage current mirror and level shifted low voltage current mirror.

VI. CONCLUSION

The purpose of this work was to improve the dynamic range, bandwidth and to reduce the power dissipation in CMOS current mirror operating on a supply voltage of 1V. Extensive simulations and optimization were carried out to meet these objectives. Level shifted low voltage CMOS current mirror topology was selected and optimized to get the desired results by varying dimensions of transistors and biasing voltages. Dynamic range has improved by a factor of 800µA and bandwidth has improved by more than 160 MHz as compared to the reference work. The power dissipation has improved by more than 40%.

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