

Modelling of Controlled On-Time Boost Power-Factor-Correction Converter by Linearising the Large-Signal Average Model

Soumya Sunny, Rency Roy, Priyanka K, E Escalin Preethi, Kokila R

Abstract: *Controlled on time boost power-factor-correction converter is modelled using large-signal transient behaviour of the circuit. Large-signal model is linearised to form small signal model.*

Index Terms: *Large-signal model, controlled on-time boost power factor-correction converter, small-signal model.*

I. INTRODUCTION

The controlled on-time boost PFC circuit [4] is widely used in low power applications [1], [2]. However models predicting exact behaviour of the converter are not available while it comes to predict phase characteristics of the PFC circuit. Low frequency model [3] is used in predicting the behaviour of the converter which is not accurate. Accordingly, a control design based on the low-frequency model can overestimate the phase margin of the PFC circuit. This inaccuracy of the low-frequency model becomes increasingly consequential when the control bandwidth of the PFC circuit expands with the employment of auxiliary means of removing low frequency ripple from the output voltage, for example, the addition of a notch filter in the control loop [2].

This paper proposes a new small signal model which overcomes the inaccuracy of previous models of the converter. First, an average model is proposed that predicts the averaged time-domain behaviour of the PFC circuit. Secondly, a small-signal model that overcomes the inaccuracy of the existing low-frequency model is obtained by linearizing the average model. Finally, the ac dynamics of the PFC circuit are investigated using this small-signal model. It will be shown that the control-to-output transfer function of the PFC circuit contains a pole-zero pair that is located at the same distance from the origin yet on opposite sides of the plane. This pole-zero pair causes an additional 180 phase delay and critically influences the phase characteristics of the PFC circuit.

A. Large Signal Model

Large-signal modelling is a common analysis method used in electrical engineering to describe nonlinear devices in terms of the underlying nonlinear equations. In circuits containing nonlinear elements such as transistors, diodes, and vacuum tubes, under "large signal conditions",

AC signals have high enough magnitude that nonlinear effects must be considered. "Large signal" is the opposite of "small signal", which means that the circuit can be reduced to a linearized equivalent circuit around its operating point with sufficient accuracy.

Small-signal modelling is a common analysis technique in electrical engineering which is used to approximate the behaviour of nonlinear devices with linear equations. This linearization is formed about the DC bias point of the device (that is, the voltage/current levels present when no signal is applied), and can be accurate for small excursions about this point.

A small signal model takes a circuit and based on an operating point (bias) and linearizes all the components. Nothing changes because the assumption is that the signal is so small that the operating point (gain, capacitance etc.) doesn't change.

A large signal model on the other hand takes into account the fact that the large signal actually affects the operating point and takes into account that elements are non-linear and that circuits can be limited by power supply values. A small signal model ignores simultaneous variations in the gain and supply values.

A large signal is a DC signal (or an AC signal at a point in time) (one or more orders of magnitude larger than the small signal) used to analyse a circuit containing non-linear components and calculate an operating point (bias) of these components. A small signal is an AC signal superimposed on a circuit containing a large signal. In analysis of the small signal's contribution to the circuit, the non-linear components are modelled as linear components.

II. LARGE-SIGNAL AVERAGE MODEL

Fig. 1(a) shows a schematic diagram of the controlled on-time boost PFC circuit [1], [2]. Fig. 1(b) shows the major waveforms of the PFC circuit assuming that the rectified line voltage v_s , output voltage v_o , and control voltage v_c , remain constant within each switching period T_s . Initially, the PFC circuit assumes an on-time operation where the MOSFET is on and the ramp signal, v_{ramp} , increases

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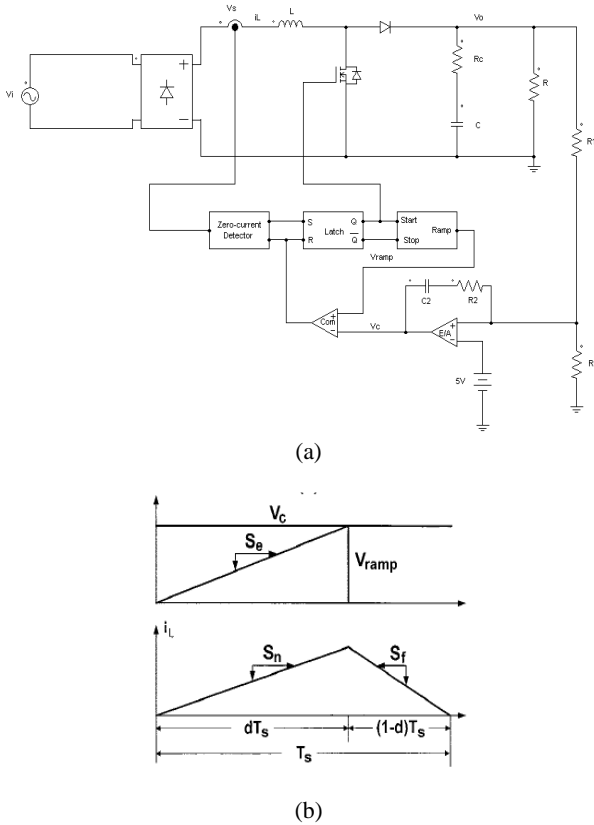


Fig. 1. Controlled on-time boost PFC circuit (a) Schematic diagram. (b) Major waveforms: s_e represents the slope of the ramp signal, s_n is the on-time slope of the inductor current, and s_f is the off-time slope of the inductor current.

with the slope of s_e . When the v_{ramp} reaches the control voltage v_c , the comparator resets the latch and the PFC circuit commences the off-time operation by turning the MOSFET off and resetting the v_{ramp} . When the inductor current is reduced to zero, the zero-current detector sets the latch and the PFC circuit resumes its on-time operation.

A. Average Model for Power Stage

First formulate a set of time-averaged equations for the voltages and currents associated with the sub-circuit that alters its structure during each switching interval. The instantaneous voltage across the inductor $v_{cb}(t^*)$ can be given as

$$V_{cb}(t^*) = \begin{cases} V_{ca}(t^*) & -t \leq t^* < t + dT_s \\ V_{ca}(t^*) - V_{pa}(t^*) & -t + dT_s \leq t^* < t + T_s \end{cases} \quad (1)$$

The time-averaged expression for the voltage across the inductor can be given by

$$\begin{aligned} V_{cb}(t) &= \frac{1}{T_s} \left[\int_t^{t+dT_s} v_{ca}(t^*) dt^* \right] + \frac{1}{T_s} \left[\int_{t+dT_s}^{t+T_s} (v_{ca}(t^*) - v_{pa}(t^*)) dt^* \right] \\ (2) \\ &= \frac{1}{T_s} [V_{ca}(t)[t+dT_s-t]] + \frac{1}{T_s} [V_{ca}(t)[t+T_s-t-dT_s] - V_{pa}(t)[t+T_s-t-dT_s]] \\ &= \frac{1}{T_s} [V_{ca}(t)[dT_s]] + \frac{1}{T_s} [V_{ca}(t)[T_s-dT_s] - V_{pa}(t)[T_s-dT_s]] \\ &= dV_{ca}(t) + V_{ca}(t)(1-d) - V_{pa}(t)[1-d] \\ &= V_{ca}(t) - V_{pa}(t)(1-d) \end{aligned} \quad (3)$$

The averaged expression for the voltage across the switch

can be given by

$$V_{ba}(t) = V_{bc}(t) + V_{ca}(t) \quad (4)$$

$$V_{ba}(t) = (1-d)V_{pa}(t) - V_{ca}(t) + V_{ca}(t) \quad (5)$$

$$V_{ba}(t) = (1-d)V_{pa}(t) \quad (6)$$

By applying the power balance condition to Fig. 2, it follows that

$$V_{ba}(t)I_L(t) = V_{pa}(t)I_p(t) \quad (7)$$

which can be simplified as

$$(1-d)V_{pa}(t)I_L(t) = V_{pa}(t)I_p(t)$$

$$(1-d)I_L(t) = I_p(t)$$

$$I_p(t) = (1-d)I_L(t) \quad (7)$$

where $I_p(t)$ and $I_L(t)$ represent the time-averaged value of the associated currents. Equations (5) and (7) describe the time-averaged dynamics of the sub-circuit.

B. Average Model for Modulator

Referring to Fig. 1(b), the slope of the ramp signal can be written as

$$s_e = \frac{v_c}{dT_s} \quad (8)$$

and the on-time slope and off-time slope of the inductor current can be given as

$$s_n = \frac{v_s}{L} \quad (9)$$

$$s_f = \frac{v_o - v_s}{L} \quad (10)$$

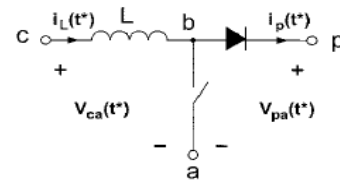


Fig. 2. Sub-circuit consisting of active-passive switch pair and inductor.

It can be seen from Fig. 1(b) that

$$s_n dT_s = s_f (1-d)T_s \quad (11)$$

which simplifies to

$$(s_f + s_n)d = s_f \quad (12)$$

Referring to Fig. 1(b), the time-averaged value of the inductor current can be found to be

$$s_f + s_n = \frac{v_o}{L}$$

$$\frac{v_o}{L} d = s_f$$

$$s_n = \frac{v_o}{L} - s_f$$

$$= \frac{v_o}{L} - \frac{v_o}{L} d$$

$$= \frac{v_o}{L} (1-d)$$

$$T_s = \frac{v_c}{ds_e}$$

$$i_L = 0.5 \left(\frac{V_o}{L} (1-d)d^2 + \frac{V_o}{L} d(1-d)^2 \right) T_s \quad (13)$$

By incorporating (8)–(10) and (12) into (13) and simplifying the resulting equation, the following equation can be obtained:

$$\begin{aligned} v_o d[(1-d)d + (1-d)^2] &= \frac{i_L L}{0.5 T_s} = \frac{2 i_L L d s_e}{v_c} \\ v_o d[(1-d)d + (1-d)^2] - \frac{2 s_e i_L L d}{v_c} &= 0 \\ v_o d[d - d^2 + 1 + d^2 - 2d] - \frac{2 s_e i_L L d}{v_c} &= 0 \\ v_o d[-d + 1 - \frac{2 s_e i_L L}{v_o v_c}] &= 0 \\ v_o d[d + \frac{2 s_e i_L L}{v_o v_c} - 1] &= 0 \end{aligned} \quad (14)$$

which gives an expression for the duty cycle as

$$d = \left[1 - \frac{2 s_e i_L L}{v_o v_c} \right] \quad (15)$$

III. SMALL- SIGNAL MODELLING AND ANALYSIS

A small-signal model of the PFC circuit can be obtained, in principle, by linearizing the average model. One simple solution to this problem is to consider PFC circuits as dc-to-dc converters with an equivalent dc input that corresponds to the rms value of the rectified line voltage.

By adapting the aforementioned approximation to the average model developed in the previous section, this section presents a small-signal model for the controlled on-time boost PFC circuit.

A. Small-Signal Model for Power Stage

Assuming the input of the power stage is a dc voltage identical to the rms value of the rectified line voltage, (5) and (7) can be linearised to produce equations relating the ac components of the circuit variables

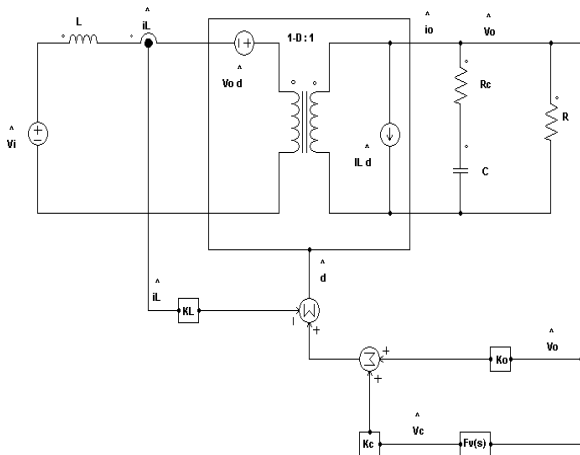


Fig. 3. Small-signal circuit model of PFC circuit: $F_v(s) = (1 + sC_2R_2) / sC_2R_1$, $K_c = (1-D) / V_c$, $K_o = (1-D) / V_o$, and $K_L = 2Ls_e / (V_c V_o)$.

$$v_{ba} = (1-D)v_{pa} - V_{pa} d \quad (16)$$

$$i_p = (1-D)i_L - I_L d \quad (17)$$

A. Small-Signal Model for Modulator

By linearizing (15), the small-signal duty ratio, can be expressed as a linear combination of the small-signal components of the circuit variables associated with the

average model of the modulator

$$d = \frac{1-D}{V_c} v_c + \frac{1-D}{V_o} v_o - \frac{2Ls_e}{V_c V_o} i_L \quad (18)$$

with

$$V_c = \frac{2Ls_e I_L}{(1-D)V_o} \quad (19)$$

B. Small-Signal Model for Modulator

An analytical expression for the control-to-output transfer function of the PFC circuit is derived, thereby, addressing the difference between the new transfer function and the existing low-frequency model. From the small-signal model of Fig. 3, the following equations can be easily seen:

$$v_o = \frac{R(1+sCR_c)}{1+sC(R+R_e)} \hat{i}_o \quad (20)$$

$$i_o = (1-D)i_L - \frac{V_o}{R(1-D)} d \quad (21)$$

$$i_L = \frac{V_o}{sL} d - \frac{(1-D)}{sL} v_o \quad (22)$$

Equation (18) can be rewritten as

$$d = \frac{1-D}{V_c} v_c + \frac{1-D}{V_o} v_o - \frac{R(1-D)^2}{V_o} i_L \quad (23)$$

Equations (20)–(23) can be simultaneously solved to yield an expression for the control-to-output transfer function:

$$v_o = \frac{R(1+sCR_c)}{1+sC(R+R_c)} \left[(1-D) \left\{ \frac{V_o}{sL} d - \frac{(1-D)}{sL} v_o \right\} - \frac{V_o}{R(1-D)} d \right]$$

$$v_o = \frac{R(1+sCR_c)}{1+sC(R+R_c)} \left[\left\{ (1-D) \frac{V_o}{sL} - \frac{V_o}{R(1-D)} \right\} d - \frac{(1-D)^2}{sL} v_o \right]$$

$$\frac{1+sC(R+R_c)}{R(1+sCR_c)} v_o = (1-D) \frac{V_o}{sL} d - \frac{(1-D)^2}{sL} v_o - \frac{V_o}{R(1-D)} d$$

$$\left[\frac{1+sC(R+R_c)}{R(1+sCR_c)} \right] + \frac{(1-D)^2}{sL} v_o = \left[(1-D) \frac{V_o}{sL} - \frac{V_o}{R(1-D)} \right] d$$

$$= \left[\frac{(1-D)^2 R V_o - sL V_o}{sLR(1-D)} \right] d$$

$$= \left[\frac{(1-D)^2 R - sL}{sLR(1-D)} \right] V_o d$$

$$d = \left[\frac{1-D}{V_o} \right] \left[\frac{sL(1+sC(R+R_c)) + (1-D)^2 R(1+sCR_c)}{sLR(1+sCR_c)} \right] \left[\frac{sLR}{R(1-D)^2 - sL} \right] v_o$$

$$d = \left[\frac{1-D}{V_o} \right] \left[\frac{sL + s^2 LC(R+R_c) + (1-D)^2 R(1+sCR_c)}{(1+sCR_c)(R(1-D)^2 - sL)} \right] v_o$$

$$d = \frac{1-D}{V_c} v_c + \frac{1-D}{V_o} v_o - \frac{R(1-D)^2}{V_o} \left[\frac{V_o}{sL} d - \frac{1-D}{sL} v_o \right]$$

$$d \left[1 + \frac{R(1-D)^2 V_o}{V_o sL} \right] = \frac{1-D}{V_c} v_c + \frac{1-D}{V_o} v_o + \frac{R(1-D)^2 (1-D)}{V_o sL} v_o$$

$$d \left[\frac{sL + R(1-D)^2}{sL} \right] = \frac{1-D}{V_c} v_c + \left[\frac{1-D}{V_o} + \frac{R(1-D)^3}{V_o sL} \right] v_o$$

$$= \frac{1-D}{V_c} v_c + \left[\frac{sL(1-D) + R(1-D)^3}{V_o sL} \right] v_o$$

$$d \left[\frac{sL + R(1-D)^2}{sL} \right] = \frac{1-D}{V_c} v_c + \frac{(1-D)}{V_o} \left[\frac{sL + R(1-D)^2}{sL} \right] v_o$$

$$\left[\frac{sL + R(1-D)^2}{sL} \right] \left[\frac{1-D}{V_o} \left[\frac{sL + s^2 LC(R+R_c) + (1-D)^2 R(1+sCR_c)}{(1+sCR_c)(R(1-D)^2 - sL)} \right] \right] v_o =$$

$$\frac{1-D}{V_c} v_c + \frac{(1-D)}{V_o} \left[\frac{sL + R(1-D)^2}{sL} \right] v_o$$

$$\left[\frac{sL + R(1-D)^2}{sL} \right] \left[\frac{1-D}{V_o} \left[\frac{sL + s^2 LC(R+R_c) + (1-D)^2 R(1+sCR_c)}{(1+sCR_c)(R(1-D)^2 - sL)} - 1 \right] \right] v_o$$

$$= \frac{1-D}{V_c} v_c$$

$$\left[\frac{sL + R(1-D)^2}{(R(1-D)^2 - sL)} \right]$$

$$\left[\frac{sL + s^2 LC(R+R_c) + (1-D)^2 R(1+sCR_c) - (1+sCR_c)(R(1-D)^2 - sL)}{sL(1+sCR_c)} \right]$$

$$= \frac{V_o}{V_c} \frac{v_c}{v_o}$$

$$\left[\frac{sL + R(1-D)^2}{(R(1-D)^2 - sL)} \right]$$

$$\left[\frac{sL + s^2 LCR + s^2 LCR_c + R(1-D)^2(1+sCR_c) - R(1-D)^2(1+sCR_c) + sL(1+sCR_c)}{sL(1+sCR_c)} \right]$$

$$= \frac{V_o}{V_c} \frac{v_c}{v_o}$$

$$\left[\frac{R(1-D)^2 + sL}{(R(1-D)^2 - sL)} \right] \left[\frac{sL + s^2 LCR + s^2 LCR_c + sL + s^2 LCR_c}{sL(1+sCR_c)} \right] = \frac{V_o}{V_c} \frac{v_c}{v_o}$$

$$\left[\frac{1 + s \frac{L}{R(1-D)^2}}{1 - s \frac{L}{R(1-D)^2}} \right] \left[\frac{2sL + 2s^2 LCR_c + s^2 LCR}{sL(1+sCR_c)} \right] = \frac{V_o}{V_c} \frac{v_c}{v_o}$$

$$\left[\frac{1 + s \frac{L}{R(1-D)^2}}{1 - s \frac{L}{R(1-D)^2}} \right] \left[\frac{2 + 2sCR_c + sCR}{(1+sCR_c)} \right] = \frac{V_o}{V_c} \frac{v_c}{v_o}$$

$$\frac{v_o}{v_c} = \frac{V_o}{V_c} \left[\frac{1 + sCR_c}{2 + sC(R + 2R_c)} \right] \left[\frac{1 - s \frac{L}{R(1-D)^2}}{1 + s \frac{L}{R(1-D)^2}} \right]$$

$$\frac{v_o}{v_c} = \frac{V_o}{V_c} \left[\frac{1 + sCR_c}{2 + sC(R + 2R_c)} \right] F_{pz}(s) \quad (24)$$

where

$$F_{pz}(s) = \frac{1 - s \frac{L}{R(1-D)^2}}{1 + s \frac{L}{R(1-D)^2}} \quad (25)$$

The $F_{pz}(s)$, a polynomial consisting of the right-half-plane (RHP) zero and left-half-plane pole (LHP) located at the same frequency, does not affect the magnitude of v_o/v_c yet introduces a 180 phase delay around $\omega_{pz} = R(1-D)^2/L$. The presence of $F_{pz}(s)$ in v_o/v_c is the unique characteristic of the controlled on-time boost PFC circuit, which is not found in other PFC circuits or dc-to-dc converters. It can be shown

that the existing low-frequency model [3] implicitly assumes $F_{pz}(s) = 1$, and thereby incorrectly predicts the phase response of the transfer function.

IV. CONCLUSION

An accurate model for on time boost power-factor-correction converter is presented which is helpful in predicting exact phase characteristics of the PFC circuit. Large signal model of the PFC circuit is linearised to get a small signal model which is useful in overcoming disadvantages of the existing low frequency model.

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