International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-8 Issue-4, April 2019

Test and Analysis of High-Performance Microprocessor Through Power Binning Method

S.Rooban, K.Sarath Kumar, K. Ravi Shankar, N. Udaya Bhaskara Rao

Abstract: Structuring superior frameworks with high return under parameter varieties has brought genuine plan difficulties up in nanometer innovations. With expanding process variety, binning has turned into a vital method to improve the estimations of manufactured chips, particularly in elite microchips where straightforward locks are broadly utilized. In this examination, we center around self-testing and execution binning. We make the accompanying commitments. To begin with, we propose a Built in self-testing strategy , in manufacture of a chip diverse parameters changes in execution of microchip distinctive outstanding burdens contrast for various items (PCs, mobile's....etc.). BIST basically comprises of straight criticism move register square and different information signature register square (yield reaction compactor). At that point, an execution binning strategy dependent on basic at-speed defer testing is created for strong frameworks to incredibly spare the binning cost, and a versatile clock arrangement method is proposed for yield improvement.

Index Terms*: *BIST, LFSR, MISR.

I. INTRODUCTION

Built-in-self test (BIST) is used to test the chip itself. In fabrication of a chip different parameters varies and infield execution of microprocessor different workloads differ for different products (laptops, mobile's….etc.). BIST mainly consists of linear feedback shift register block and multiple input signature register block (output response compactor).

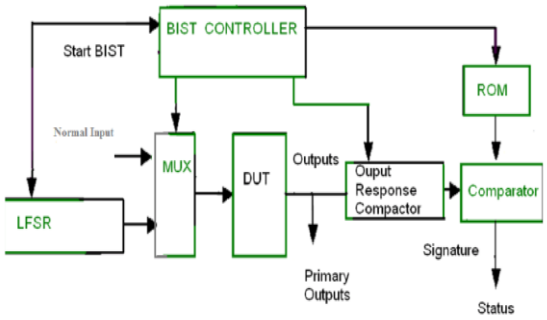

Fig 1 BIST Architecture

Linear feedback shift register (LFSR) consists of flip flops and x-or gate. LFSR generates test vectors. And the test vectors are applied on the internal nodes of the circuit that to be tested. Multiple shift register is a form of LFSR and it compares the input response with the output response. In fabrication of chip different parameters are taken into consideration like size, cost, power consumption…etc. To decrease the power consumption the size of the chip or the blocks of microprocessor should be reduce .so, to reduce the blocks we use 8 bit ripple carry adder. While implementing this we have the check the chip area that it occupied, power consumed during the in-field execution. As technology is increasing the density of IC's and performance are increasing. Notwithstanding, such advantages are joined by a noteworthy increment in power utilization and ,subsequently, chip's temperature, which commands the advancement of complex power the executives strategies to stay away from lasting harm of the chip, or critical decreases of the charge self-sufficiency of convenient gadgets Additionally, due to a normal, persistent increment with innovation scaling of procedure parameter varieties happening amid creation, huge varieties (chip by chip) of the power devoured by the manufactured microchips, regarding what expected by structure Performance (or speed) binning alludes to test techniques to decide the most extreme working recurrence of a processor. To test the imperfections MISR (various information signature register) it give the reaction of the circuit, on the off chance that it offer any mistake, at that point then we will in general consider that the circuit has blame. As innovation is expanding the thickness of IC's and execution are expanding. In any case, such advantages are joined by a huge increment in power utilization and ,subsequently, chip's temperature, which commands the improvement of complex power the board strategies to stay away from perpetual harm of the chip, or critical decreases of the charge self-rule of versatile gadgets Additionally, due to a normal, ceaseless increment with innovation scaling of procedure parameter varieties happening amid manufacture, noteworthy varieties (chip by chip) of the power devoured by the created microchips, concerning what expected by plan Performance (or speed) binning alludes to test techniques to decide the most extreme working recurrence of a processor. On account of uniprocessors, the execution of a processor is emphatically associated with its recurrence of activity. Therefore, processors have generally been binned by recurrence. In any case, for chip multiprocessors, the proper binning measurements are significantly less clear because of two fundamental contemplations On the off chance that binning is finished by the most elevated basic working recurrence all things considered.

Manuscript published on 30 April 2019.
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(one clear expansion to the uniprocessor binning metric), great execution connection of the binning metric would just be seen when the most extreme working frequencies of all centers are fundamentally the same as. We conjecture that this supposition won't remain constant later on dependent on the accompanying perceptions.

The second motivation behind why binning measurements may should be rethought for multi-center processors is that a decent binning metric ought not just associate well with the most extreme execution of the chip however ought to likewise have satisfactory time overhead for the binning procedure.

As transistors are decreased in size, it winds up harder controlling varieties in gadget parameters, for example, channel length, entryway width, oxide thickness, and gadget limit voltage.These vacillations in the process parameter conveyances or just process varieties cause expanded changeability in circuit execution and are probably going to be more predominant in sub-90 nm space. Indeed, even in a generally develop innovation like 130 nm, these varieties are referred to result in as much as 30% reduction in most extreme recurrence and 500% expansion in spillage control [18]. For more current advancements, these varieties can be much higher: 20-overlap increments in spillage have been accounted for 90nm. Process varieties comprise of With-in-Diode (WID) and Inter-Diode or Diode-to-Diode (D2D) parameter varieties.

II. METHODOLOGY

In this linear feedback shift registers algorithm it will generates the sequence of the binary values these values are repetitively occurred are known as the pseudo random sequences this feedback paths are constitutes exclusive-or or exclusive nor to make the random series

A. MULTIBIT LFSR BASED ALGORITHMS

In the multibit LFSR algorithm the random number generators are less cryptographic security applications but it can be possible by the shifted n bits in one cycle and generate the new random series by using the state space methodology.

*B.*IMPLEMENTATION OF MULTIBIT LFSR ALGORITHM

In the multibit LFSR algorithm 8 bit simple polynomial has been generated . The pseudo random pattern generator is used in the cryptographic application by using the (FPGA) field programmable gate array there is the reconfigurable logic blocks and I/O blocks .

C. THEORETICAL ANALYIS

They are two forms of built-in-self-test they are logic built-in self-test(LBIST) and memory built-in-self-test(MBIST) .To achieve our goal , during the power characterization phase, we induce test vectors on the inward hubs of the successive circuits of a microchip. While checking the chip of various sort of items outstanding tasks at hand fluctuates starting with one item then onto the next items. Our methodology misuses the output based Logic Built-In Self-Test (LBIST) structures (habitually received to perform smaller scale process or at-speed testing) to apply to the chip's successive circuits(CUTs)proper test vectors equipped for initiating on the CUTs inward hubs in the field by the execution of outstanding burdens for various items. As likewise examined in, we trust this is a compelling method to describe the power that every single manufactured chip will devour in the field, at a moderate expense. We will demonstrate that, for the thought about square of the microchip, test vectors do the trick to acquire an exact power portrayal. In BIST test vectors are produced by Pseudo irregular example generator (PRPG)and all tasks occurring amid output based LBIST are controlled by the BIST Controller.

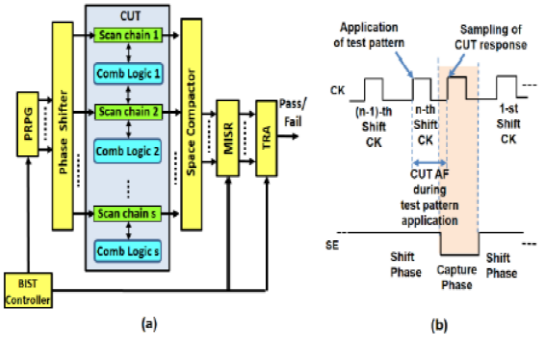

Fig 2 LBIST Architecture & Timing Diagram.

It ought to be noticed that, the selection of LBIST plans for the diverse squares making the chip is progressively considered as a productive technique to lessen at-speed test cost, and to improve test quality. Thus, a few complex multicore chips present a self-ruling LBIST engineering for each successive square, just as a self-governing MBIST (memory BIST) for each SRAM [22]. Hence, so as to give a precise portrayal of the entire chip control utilization, our methodology can be utilized to control the consecutive squares of the microprocessor (by misusing their autonomous LBIST structures), together with the procedure in the inserted memory squares. We propose programming usage. In our methodology we execute the 8 bit swell convey viper to decrease territory overhead, which for thinking of some as a component of ALU square of chip as 8 bit swell convey snake. It ought to be noticed that, the appropriation of LBIST plans for the distinctive squares forming the chip is progressively considered as a proficient methodology to lessen at-speed test cost, and to improve test quality. Therefore, a few complex multicore chips present a self-sufficient LBIST design for each consecutive square, just as a self-governing MBIST (memory BIST) for each SRAM . In this way, so as to give a precise portrayal of the entire chip control utilization, our methodology can be utilized to control the successive squares of the microprocessor (by misusing their autonomous LBIST structures), together with the system in the implanted memory squares. We propose programming usage. In our methodology we actualize the 8 bit swell convey snake to diminish zone overhead, which for thinking of some as a major aspect of ALU square of microchip as 8 bit swell convey viper.

D. BIST TECHNIQUE

Built-In-Self-Test is a methodology of fusing the handiness of a modified test system onto a chip. It is a Design for Test strategy in which testing (test age and test application) is cultivated through implicit equipment highlights.

The general BIST engineering has a BIST test controller which controls the BIST circuit, test generator which creates the test address arrangement, reaction check as a comparator which contrasts the memory yield reaction and the normal right information and a CUT. We have used LFSR to produce the test vectors. The BIST controller can be acknowledged by either organized premise as a Finite State Machine (FSM), microcode controller or processor-based yield chain AF decline or addition is required(AF Red/Inc.); a banner showing the pined for entirety of sweep chain AF decrease/increase (AF amount).Our approach similarly delivers a control banner (TM) to trigger the ATE control estimation.

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III.EXPERIMENTAL RESULTS

A.BIST RTL VIEW

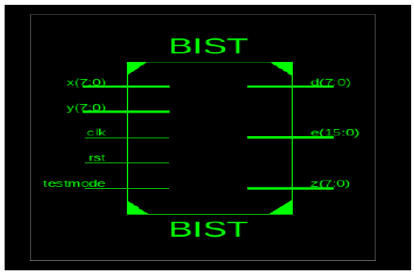

Fig 3 RTL View Of BIST

The top-level Verilog module is created for BIST by giving the inputs are x(7:0),y(7:0),clk, rst, and test mode and output ports as d(7:0),e(150)and z(7:0)

The output d(7:0) is the output of the MISR the compares the fault value of the microprocessor and it simulates the results as the clock becomes zero it implies that the microprocessor is not working well. The output e(15:0) is the output of the LFSR as they are the test vectors that are given to the 8 bit ripple carry adder. The z(7:0) is the output response of 8 bit ripple carry furthermore, it is compacted by the MISR and MISR contrasts and the first reaction. The source record containing the LFSR module shows in the Workspace, and the BIST shows in the Sources tab, as appeared as follows:

B.LFSR RTL VIEW

Fig 4 RTL view of LFSR

The top level Verilog module is created for LFSR by giving the input ports as clock and output ports as e(15:0) which is of 16bit.The output of LFSR is stored in register and the output generates by the LFSR are nothing but the test vectors.. The BIST controller gives the test mode and the normal if the test mode is given then the BIST works in test mode otherwise it work in normal mode.

C. 8BIT RIPPLE CARRY ADDER

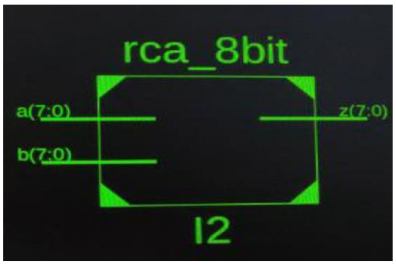

Fig 5 RTL View Of 8 Bit Ripple Carry Adder

D.MISR RTL VIEW

Fig 6 RTL View Of MISR

E.8BIT RIPPLE CARRY ADDER INTERNAL VIEW

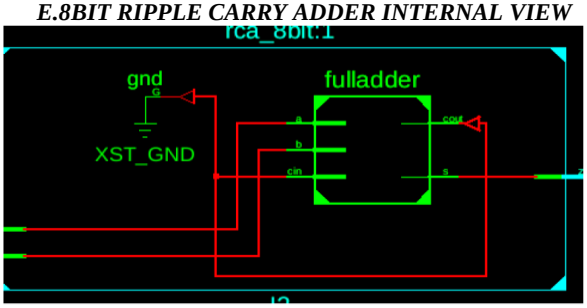

Fig 7 Internal RTL View Of Ripple Carry Adder

F.SIMULATION RESULTS

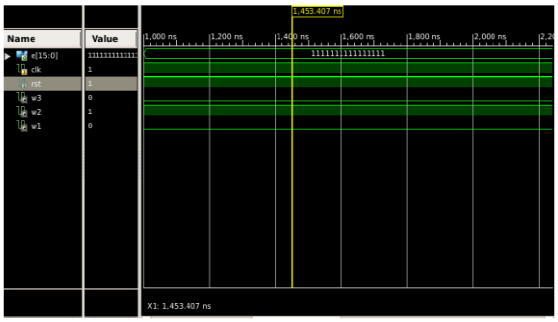

Fig 8 timing diagram of LFSR

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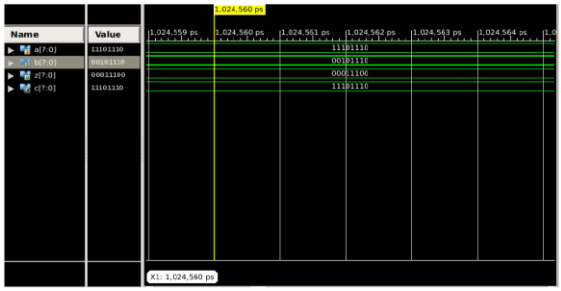

Fig 9 Timing Diagram Of rca_8bit

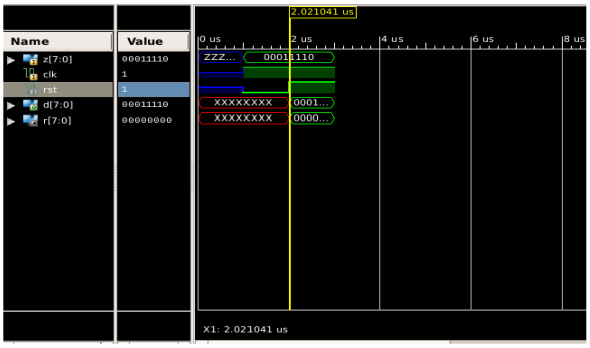

Fig 10 Timing Diagram Of MISR

G.OUTPUT

The BIST must work effectively with an information clock recurrence = 260MHz to 289MHz. The information will be legitimate 5.34 ns before the rising edge of CLOCK. The yield must be substantial 7.408 ns after the rising edge of CLOCK. The plan necessities relate with the qualities underneath. Fill in the fields in the Initialize Timing discourse box with the accompanying data: Clock High Time .Clock Low Time: 1 ns. Info Setup Time: 1ns. Output Valid Delay: 8.778 ns. Starting Length of Test Bench 10000 ns **.**

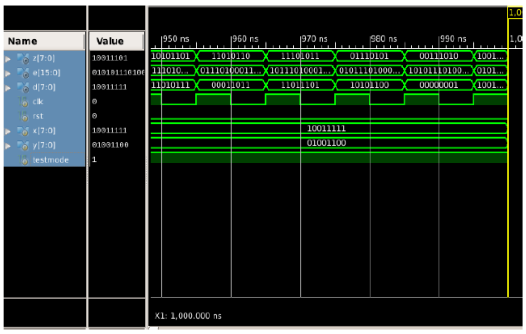

Fig 11 Timing Diagram Of BIST

H.TECHNOLOGY SCHEMATIC OF BIST

Innovation schematic is created after the advancement and focusing on period of the blend procedure which is appeared in the Fig. 8. In this Technology schematic the structure is spoken to regarding LUT's. Innovation schematic enables the creator to see an innovation level portrayal of HDL, which may assist the fashioner with discovering any plan issues.

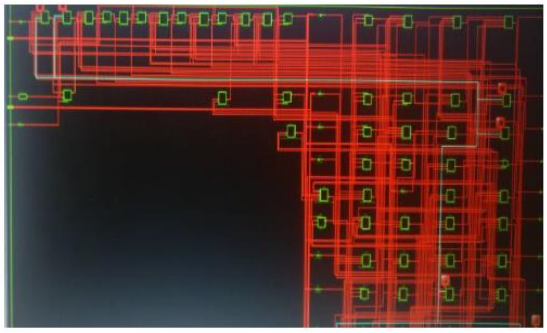

Fig 12 Technology Schematic of BIST

IV. DISCUSSION OF RESULTS

A.POWER ANALYSIS FOR BIST

The power is estimated for the BIST to test CUT (ripple carry adder). The BIST consumes 0.014W.

TABLE 1 Power analysis report

Supply Summary		Total current (A)	Dynamic current (A)	Quiescent current(A)
Source	Voltage			
Vccint		0.004	0.0000	0.004
Vccax		0.003	0.0000	0.003
Vcco25		0.001	0.0000	0.001

Supply power (W)	Total	Dynamic	Quiescent
	0.014	0.000	0.014

B.SYNTHESIS REPORT

BISTtb Project Status (10/11/2018 - 20:36:05)			
Project File:	bist.xise	**Parser Errors:**	No Errors
Module Name:	BISTtb	**Implementation State:**	Synthesized
Target Device:	xc6slx45t-2fgg484	**• Errors:**	No Errors
Product Version:	ISE 14.7	**• Warnings:**	72 Warnings (72 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	24	54576	0%
Number of Slice LUTs	44	27288	0%
Number of fully used LUT-FF pairs	11	57	19%
Number of bonded IOBs	51	296	17%
Number of BUFG/BUFGCTRLs	1	16	6%

Fig 13 Synthesis Report

V.CONCLUSION

The outputs generated by LFSR are used as a test vector. Test mode is generated by BIST controller .The test vectors are stored in the register .This test vectors are controlled by test mode. The test vector are applied on the internal nodes of 8 bit ripple carry adder. From the output wave form of BIST we conclude that when the output of MISR and 8bit ripple carry adder are compared and when the clock becomes 0 it says that the microprocessor is not good condition.

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It is of lower cost, better fault coverage, less time for implementation, if the BIST can be designed to test more structures in parallel easier customer support and capability to perform tests outside the production electrical testing environment, additional silicon area, reduced access times, additional pin (and possibly bigger package size) requirements.

VI. FUTURE SCOPE

The design we used to test and analysis the microprocessor is used to reduce the area and power consumption. In future this design is used to design the high performance chip that it takes less area and less power consumption .

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