International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-8 Issue-6, August 2019

Bare PCB inspection for Track cut, Track Short and Pad Damage using simple Image Processing Operations

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Abstract: ***In this paper most commonly occurring Bare PCB defects such as Track Cut, Track short and Pad Damages are detected by Image processing techniques. Reference PCB without having any defects is compared with test PCB having defects to identify the defects and x-y coordinates of the center of the defects along with radii are obtained using Difference of Gaussian method and location of the individual type of defects are marked either by similar color or different colors. Result Analysis includes time taken for the inspection of a single defect, multiple similar defects, and multiple different defects. Time taken is ranging from 1.674 to 1.714 seconds if the individual type of defects are marked by different colors and 0.670 to 0.709 seconds if all the identified defects are marked by the same colors.***

Keywords **: *Printed Circuit Board, Difference of Gaussian, Mean thresholding, Defect Detection, Localization***

I. INTRODUCTION

Printed Circuit boards provide Electrical conductor path for the interconnection of components and Mechanical support for the mounted components. Based on the number of layers, PCBs are classified as single-sided, double-sided and multilayer boards. Single-layer PCB contains circuits only on one side. Double-layer PCB contains the circuit on both top and a bottom layer which is mainly used for the products such as remote controls, audio equipment, car radios manufactured in high-volume with low-cost. Multilayer boards contain more than three layers and used for sophisticated industrial and consumer electronic products. Generally, two types of components are found on the PCB namely, Through-hole and surface mount. The main features of the bare PCBs includes copper tracks, pads, and holes. Copper tracks are used to link the components to form the circuit. Pads are the area on the PCB where the components are mounted to the board. Pads are of two types, through hole pads used for soldering through-hole components and surface mount pads used for soldering surface mount components. Holes are used for inserting through-hole components in PCB.

It is difficult to get 100% yield from PCB assembly and manufacturing. However, the percentage of defective PCB exponentially reduces due to the use of a wide variety of process and quality improvement techniques. In spite of these improvements, the need for bare board testing remains. The main reason to test the bare board is to block the addition of further value to the defective product. Bare board is the basic component of loaded boards, systems and final products used in the fields. If the defects are identified in bare PCB itself then cost due to that defect becomes less. If the defects are identified in the assembled board then scrapping or repair of the loaded board is approximately 10 times costlier than that of bare board. If the defective assembled board passes to system-level then cost of scrap is 100 times more than that of bare board. Similarly, if the fault found at the field then the cost of scrapping and/or servicing is 1000 times more than that of the bare board [1].

Most of the authors proposed the algorithm for defect detection and classification of Artificially created Bare PCB images which include 14 commonly known defects such as open, short, break out, pinhole, over etch, under etch, conductor too close, mouse bite, spur, missing hole, wrong size hole, missing conductor, spurious copper and excessive short[2]. These consist of well-known conventional operations such as image difference, image subtraction, image addition, and image comparison along with mathematical morphological methods for the identification of different types of defects [3]-[6].

In the proposed method, the input data used real PCBs meaning that the defects are tracked on a real PCB and all the defects are real. Reference Real Bare PCB without having any defects compared with Real Test PCB having defects to identify the presence of the defects using image processing operation. Then the location of the identified defects is extracted using Difference of Gaussian method followed by marking of defects. Section 2 of the paper discusses the types of commonly found defects and their scrap analysis and also the types of bare board testing methods presently used in various PCB industries, benefit, drawback and cost of each testing method. Section 3 describes how the defects are identified using image processing operation and localized using blob detection and marking process. Section 4 discusses the results obtained and performance analysis. Finally, conclusions are drawn.

Revised Manuscript Received on August 30, 2019.
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II. TYPES OF DEFECTS AND TESTING METHODS

During the manufacturing process, there are some defects commonly found on PCB because of dust and Panel/board handling process. The major rejection of the board due to the particular defects are identified by analyzing the six months defects Pareto chart of one of the bare board manufacturing industry as shown in Table I.

Table- I: Bare PCB Defect Pareto

Sl. No	Name of the defect	Percentage of Rejection / Scrap
1	Track cut	39%
2	Scratch	25%
3	Track Short	18%
4	Pad damage	10%
5	Others	08%

According to the analysis 39 %, 25%, 18% and 10% of the scraps are due to track cut, scratch, track short and pad damage respectively. Remaining 08% of the scrap due to all other defects. This paper mainly focused on the detection of Track cut, Track short and Pad damage and addressed 67% of the total scrap.

Bare board testing methods: The two main methods used for bare board testing are Electrical testing and Nonelectrical testing [1]. Electrical testing performs only continuity and isolation testing by passing currents through conductors and applying voltages across insulators. Electrical testing can be performed either by Jig or flying probe tester. Jig tester uses the bed of nails to access the nodes of the board and check open and short of the connection. Fixture cost and development lead time of Jig tester are more expensive and longer respectively. This method takes only one minute for testing one board. Unlike the Jig tester, a flying probe tester does not require a bed of nails fixture. Instead, it contains a small number of fixed and movable probes and easily makes a test of the top and bottom layer of the board. Cost per unit is more in flying probe tester than Jig tester because it takes a longer time of around 15 minutes for a testing single board. In these type of electrical testing, the PCB board come into physical contact with a testing equipment and there may be chances of damage to the board.

Non-Electrical testing is based on the inspection process in which the PCB board does not come into physical contact with an inspection equipment and does not make any damage to the board. Visual inspection is one of the nonelectrical testing methods in that it makes use of people, good lighting environment. As the complexity of product increases, the visual inspection becomes tedious, time-consuming, expensive, and leads to excessive scrap rates. The second method of Non-Electrical testing involves computer-based visual inspection commonly referred to as Automatic optical inspection(AOI). It consists of an image capturing system that captures an image of the good board along with the board under test. Then the comparison of two images is carried out by the processing software within the AOI system to detect any faults. But the cost of AOI equipment is very high and it is difficult for small scale PCB industries to bear such costs[7]. Therefore it is necessary to develop a relatively cheaper automatic PCB inspection system. The cost of individual testing methods is as listed in Table II[8]. Hardware equipments required for implementing the proposed method are personal computer of around Rs. 50,000 and Nikon CMOS camera of around Rs. 1,50,000. The total cost is around Rs.2,00,000 which is very less compared to all other methods.

Table II: Testing Methods and its cost

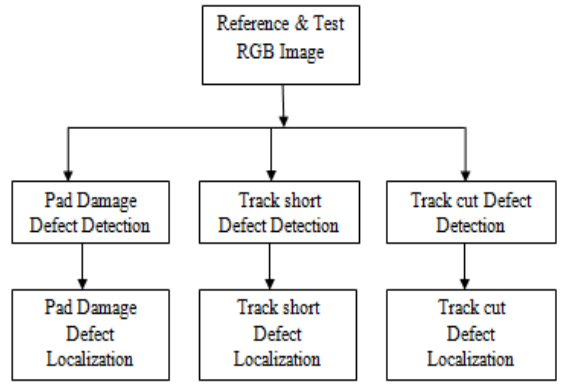
Sl. No.	Bare Board Testing methods	Cost
1	Flying Probe Test	10 lakhs
2	Jig Test	15 lakhs
3	Automatic Optical Inspection	1.2 Crore
4	Proposed method	2 lakhs

III. METHODOLOGY

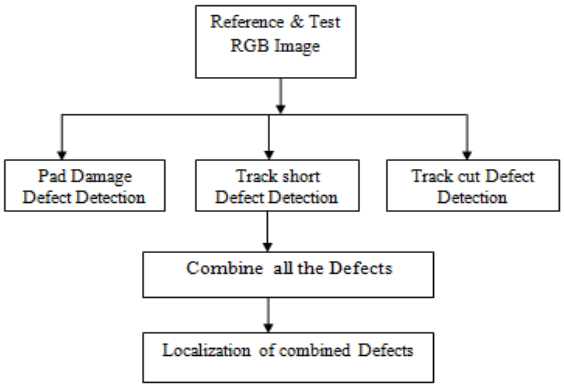
There are several techniques that have been developed to find the defect by considering the simulated PCB. Wavelet-based difference algorithm, Morphological segmentation, grayscale statistical matching techniques are adopted to handle simulated PCB [9]-[11]. In this paper, an attempt is made to identify the defect of real PCB using image processing techniques.

A. Defect Identification

The main focus in this work is the identification of three major types of defect namely Track cut, Track short and Pad damage results in 67% of the total scrap during the manufacturing process of Bare Board PCB.



(a) Individual Localization



(b) Combined Localization

Fig 1: Block diagram of Defect Identification and Localization

The Scratch defect which results in 27% of the total scrap is not addressed since this percentage varies from industry to industry and it mainly depends on the preventive measures taken during the process.

In the proposed method, the individual types of defects are identified followed by either individual type defect localization or combined defect localization as shown in Fig 1(a) and 1(b).

In case of individual localization, the location of the individual types of defects is obtained separately followed by marking in order to distinguish between the types the defects present in the board. Since localization is performed three times, it takes more time for the inspection. In case of combined localization, all the types of identified defects are combined first and then the location of the defects are obtained. In this one cannot distinguish the type of defects but it results in faster inspection since the localization is performed together.

The steps involved in the process of defect identification is depicted as in Algorithm1. The reference and test PCB are captured by the camera. The image acquired by the camera includes both foregrounds which contain PCB portion and the background. Hence extract only PCB from the background. The extracted reference and test PCB images of size MxN are properly aligned using Image registration. In the manufacturing industry defect identification of the test image should be carried out in real-time i.e., the manufactured PCB when subjected for defect identification it should be processed within a minimum computational time. Therefore the input image is downscaled to m x m so that, the number of pixels is reduced which in turn reduces the memory storage space and the processing time.

Algorithm1:DefectIdentification

Input:	I_{Ref} - Reference Image, I_T - Test Image of Size MxN ;
Output:	I_{PDD}- Pad damage defect, I_{TCD} -Track Cut defect, I_{TSD} -Track short defect ,I_{TCSP} -All defect ;
	Start
Step1:	Read_RGB_Image (I_{Ref}, I_T);
Step2:	Extract foreground(PCB) image form the background(I_{Ref}, I_T) Perform Image registration for proper alignment of reference and test image
Step3:	/*Scale down MxN sized images to mxm sized image */ Scale (I_{Ref} , I_T);
Step4:	/*Extract R,G,B components/ Channels */ (I_{Ref}^R ,I_{Ref}^G, , I_{Ref}^B) = Extract_channels(I_{Ref}); (I_T^R ,I_T^G, , I_T^B) = Extract_channels(I_T);
Step5:	/* convert Reference and Test RGB Image to Gray Scale Image */ (I_{Ref_gray} , I_{T_gray}) = RGB_to_Gray (I_{Ref}, I_T);
Step6:	/*Convert R, B components and Gray scale image of test and reference image to binary form individually */ (R_{Ref_bin} , B_{Ref_bin}) = Binary_conversion(I_{Ref}^R, I_{Ref}^B); (R_{T_bin} , B_{T_bin}) = Binary_conversion(I_T^R, I_T^B); (I_{Ref_bin} , I_{T_bin}) = Binary_conversion(I_{Ref_gray}, I_{T_gray});
Step7:	/*Invert R components and gray scale image of test and reference image in binary form individually excluding B component */ ($R_{Ref\_bin}^1$, $R_{T\_bin}^1$) = Invert (R_{Ref_bin}, R_{T_bin}); ($I_{Ref\_bin}^1$, $I_{T\_bin}^1$) = Invert (I_{Ref_bin}, I_{T_Bin});

Step8:	/*Subtract */
	for i: 0 to m-1 do
	for j: 0 to m-1 do
	$I_{PDD} = R_{Ref\_bin}^1(i,j) - R_{T\_bin}^1(i,j)$;
	$I_{TCD} = I_{Ref\_bin}^1(i,j) - I_{T\_bin}^1(i,j)$;
	$I_{TSC} = B_{Ref\_bin}(i,j) - B_{T\_bin}(i,j)$;

Step9:	/* Combine all the defects*/ I_{TCSP} = Sum(I_{PDD} , I_{TCD} , I_{TSC})
	Stop

In order to classify the test image, pixel-wise comparison with the reference image is required. The comparison should be such that, the difference between the test image and the reference image should be properly recognized. This requires the features present in the images to be effectively highlighted. It is well known that every color image is composed of Red, Green, and Blue (RGB) components or channels. Every channel can be considered as a separate image and each of them carries different information. Hence Instead of processing original color image, splitting the RGB into separate channels and processing of individual channel would contribute in highlighting the various features in the image[12]. The given PCB input image consists of background in dark green color, track in light green color and pads in silver color. In the test PCB, if there is a light green color instead of dark green color, then it represents the track short defects, dark green color instead of light green color represents track cut defect and also dark green color instead of silver color represents the pad damage defect. Each of these PCB features can be extracted by splitting the input images and it definitely helps in defect identification through comparison.

Comparison of the image requires the elimination of background features. therefore all the components are converted to binary form so that,

track and pad get highlighted followed by Inversion of the binary component for the elimination of the background. The differences found between the Inversion of the binary R component of reference and test PCB image are mainly due to pad damage defects involved in the inspected PCB. Similarly, the differences found between the Inversion of the binary gray component of reference and test PCB image are mainly due to track cut defects involved in the inspected PCB. Finally, the differences found between the binary Blue component of reference and test PCB image are mainly due to track short defects involved in the inspected PCB [13]-[15].

B. Localization of the Defects

In an Image, the bright region on the dark or dark region on bright are known as blobs. If the board contains any defect then difference images or sum of all the difference images contains white patches on black background a. The white patches are considered as blobs. The number of white patches in a difference image indicates the number of defects present in the test board. Location of these defects can be extracted using Difference of Gaussian (DoG) method. This method returns the coordinates of all the defect along with their size. For an image, the Difference of Gaussian is obtained from the difference of two Gaussian blurred images. Blurred version

Algorithm 2: Defect Localization

Input: I_{PDD}= Pad damage defect, I_{TCD} = Track Cut defect, I_{TSD} = Track Short defect of Test Image;

Output: I_{Test_M}=Test Image with highlighted Pad damage, Track_Cut and Track_short defects ;

Start

Step1: /* Extract the coordinates of the Defects*/
PD_C = Extract_defectscoordinates (I_{PDD})

Step2: /*Find the number of defects coordinates */
N_PD_C = Get_Total_Rows(PD_C)

Step3: /*Mark the location of Defects */
If N_PD_C= 0 Go to Step4
Else
For i = 1 to N_PD_C
X1i= $PD_C(cxi) - PD_C(ri)$
X2i= $PD_C(cxi) + PD_C(ri)$
Y1i= $PD_C(cyi) - PD_C(ri)$
Y2i= $PD_C(cyi) + PD_C(ri)$
I_{Test_M1}=Mark_location($I_{Test\_M1,}$ (X1i,Y1i,X2i,Y2),"Orange")
End

Step4: Repeat Steps 1 & 2 for I_{TCC} Track cut defect and also repeat step3 **if** N_TC_C **!=0** to mark the defect on I_{Test_M1} in **"RED"** Color. ***Else*** Go to next step

Step5: Repeat Steps1 & 2 for I_{TSD} Track short defect and also repeat step3 **if** N_TS_C **!=0** to mark track short defects on I_{Test_M1} in **"BLUE"** Color. ***Else*** Go to next step

Step6: /* Display count of individual type and Total defects present in the Test Image*/
Print(N_PD_C, N_TC_C, N_TS_C)
Totalcnt= $N\_PD_C + N\_TC_C + N\_TS_C$
Print(Totalcnt)
Stop

of the source image obtained by performing the convolution of the source image with the Gaussian kernel. The difference between the two blurred images gives zero crossings which represent the edges or areas of pixels that have some variation in their surrounding neighborhood that intern represents the presence of defects in the PCB board [16],[17]. The steps involved in the process of defect localization is depicted as in Algorithm2.Once the defects are identified, features of these defects such as center point of x and y coordinates (cx, cy) and size of the defect (r) are extracted first. Then the top left (x1,y1) and bottom right(x2,y2) corner of all the defects are obtained by using respective values of cx, cy, and r. Finally, the location of the defect (x1,y1,x2,y2) are marked on the corresponding test PCB .

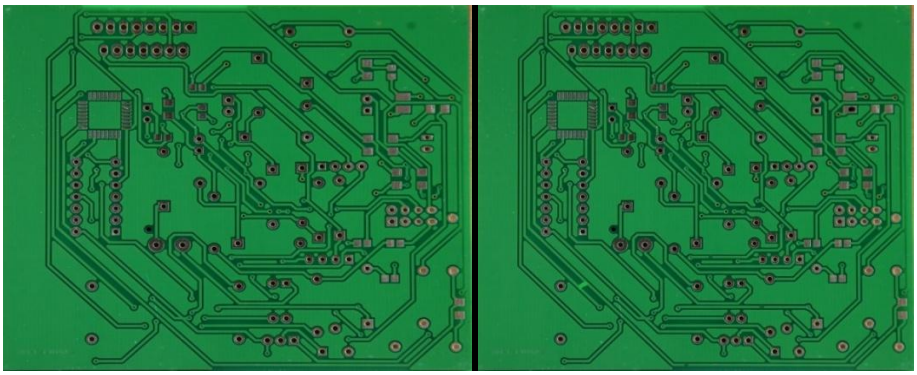
IV. EXPERIMENTAL RESULT

In our implementations, all algorithms are programmed in the Python language using Python Imaging Library (PIL), Matplotlib and Scikit-image library of Python and executed on a personal computer with an Intel(R) Core (TM) i5 4200U CPU @2.30GHz processor, 6GB memory and 64-bit operating system. The effective image size is 4177x3681 pixels and the execution time is less than 2 seconds.

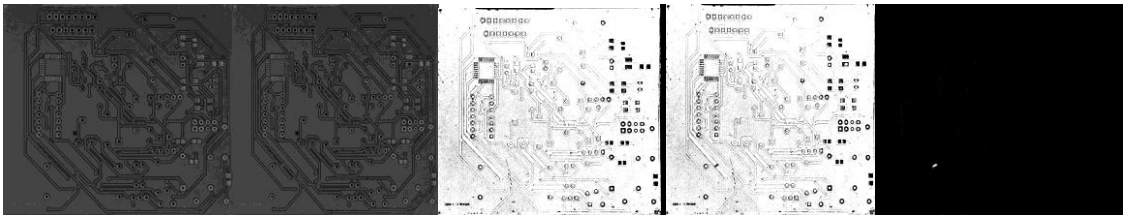
Sample PCB boards are collected from the final inspection line of Bare PCB manufacturing industry. Images of all sample good boards are captured by NIKON D810 camera with a working distance of 30cm.

Secondly, PCB boards with defects are created manually and captured. Totally 100 boards are tested by using the proposed method. Among 100 boards 50 boards are of one set and 50 boards are of another set. In each set, 15 boards are good i.e. not having any defect and 35 boards are having defects. These 35 defected boards are categorized as boards which contain only Single Defect (SD), Multiple Similar Defects (MSD-n) and Multiple Different Defect (MDD-n). Here n indicates the total number of defects in the board. In the first set there are 5 SD boards with track cut, 8 SD boards with track short, 6 SD boards with pad damage, 10 MSD-n boards with 2,3 and 4 similar defects (4 for track cut,3 for track short and 3 for pad damage) and 6 MDD_n boards having a combination of two or all the defects. In the second set, there are 2 SD boards with track cut, 2 SD boards with track short, 3 SD boards with pad damage, 12 MSD-n Boards with 2,3,4 and 5 similar defects (4 for track cut,4 for track short and 4 for pad damage) and 16 MDD_n boards having a combination of two or all the defects.

All boards of first and second set are inspected in two steps. In first steps the presence of defects are identified using algorthm1.In the second step location of the defects are extracted and marked on the test board using algoritm2.The presence of Individual type of defects such as track short, track cut and pad damage are identified separately using algorithm1. Fig 2(a) to (g) shows the output for the individual steps of Track Short Defect Detection. Fig2(g) represents the track short defect. Fig 3(a) to (g) shows the output for the individual steps of Track Cut Defect Detection. From Fig 3(e) and (f) it can observe that the image suppress the details of SMT and TH pads and highlights more on track information and thereby results in track cut defect detection. Fig3 (g) represents the track Cut defect.

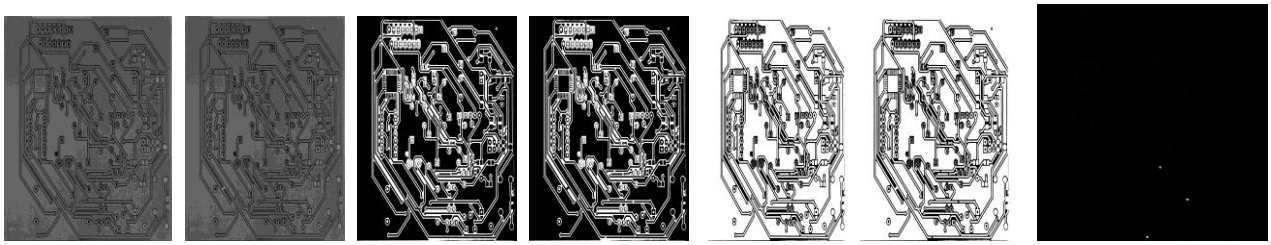


a) Reference PCB image *b)Test PCB image with one track short defect*



(c) (d) (e) (f) (g)

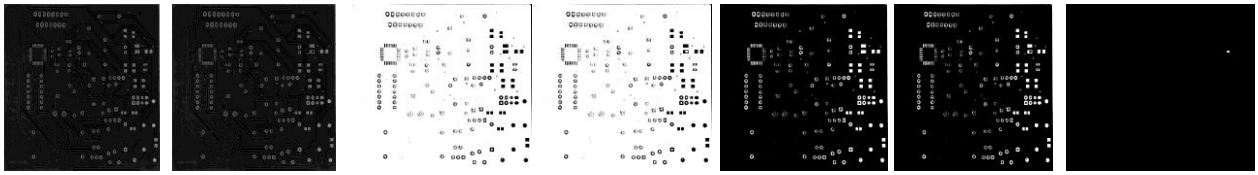
Fig 2 : Output of Track Short Defect Detection-(c) and (d) are the blue channel of Reference and Test PCB images,(e) and (f) are binary image of blue channel Reference and Test PCB images, (g) Track short defect



(a) (b) (c) (d) (e) (f) (g)

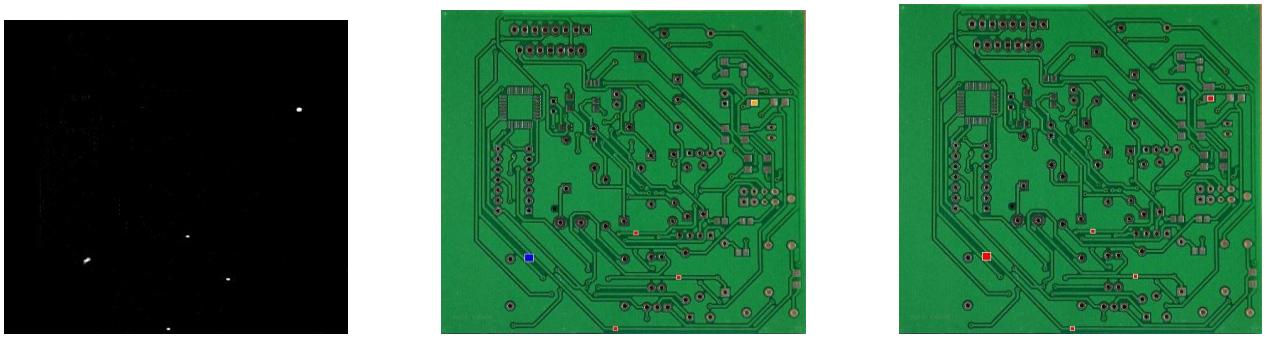
Fig 3: Output of Track Cut Defect Detection-(a) and (b) are the gray image of Reference PCB image and Test PCB image with three track cut defects,(c) and (d) are binary image of gray scale Reference and Test PCB images, (e) and (f) are the inverted image of Reference and Test PCB binary image, (g) Track cut defects

Fig 4(a) to (g) shows the output for the individual steps of Pad Damage Defect Detection. From Fig 4(c) and (d) it can observe that the image completely suppress the details of the track and highlights only SMT and TH pads and thereby results in only pad damage defect detection. Fig 4(g) represents the pad damage defect.



(a) (b) (c) (d) (e) (f) (g)

Fig 4 : Output of Pad Damage Defect Detection-(a) and (b) are the R channel of Reference PCB image and Test PCB image with pad damage defect,(c) and (d) are binary image of R channel Reference and Test PCB images, (e) and (f) are the inverted image of Reference and Test PCB binary image, (g) Pad Damage defect



(a) Combination of all defects *(b) Individual Type Defect Localization* *(c)Combined Defect Localization*

Fig 5 : Output of Defect Localization

Once the defects are identified, x and y coordinates of the center point of the defect (cx,cy) and size of the corresponding defect (r) are extracted using Algorithm2. Then the boundary of defects which includes the top left corner (x1,y1) and bottom right corner of (x2,y2) of the identified defects are calculated using the expressions x1=cx-r, y1=cy-r, x2=cx+r, and y2=cy+r. The boundary [(x1,y1), (x2,y2)] is used to mark the location of a defect in the corresponding bare board Test Image. Localization will be performed in two ways. In the first way localization is performed on individual defects IPDD, ITSD and ITCD. In the second way, all track short, track cut and pad damage defect combined to get a single output which includes all the defects (ITCSP = IPDD +ITSD+ ITCD) as shown in Figure 5(a) and then localization will be performed on Combined defects ITCSP. In Individual type of defect localization different colors can be used to show the location of defect since localization is performed separately on individual types of defects. Blue, red and orange color marking is used to indicate the location of track short, track cut and pad damage defects respectively as shown in Fig 5(b). But in Combined defect localization, only one color can be used to show the location of all the defects as shown in Fig 5(c). The boundary of defects [(x1,y1),(x2,y2)] are calculated for all 100 boards. Table III includes information about the x-coordinate of the center of the defect Cx, y-coordinate of the center of the defect Cy, radii of the defect r and boundary of the defects[(x1,y1),(x2,y2)] for 15 boards.

Performance Analysis: Performance Analysis of individual type defect localization and combined defect localization are tabulated as shown in Table IV and Table V respectively. Inspection process of both will start by reading the reference board image (golden board) and perform the preprocessing operations such as resizing, extraction of R band, B band and grayscale of golden board image, conversion of R band , B band and grayscale to a binary image. The preprocessed data of the reference image are stored in memory. This is a one-time process since the same reference board will be used for testing all the test board. Time taken for this will be 320.27msec and it is represented by RI_RPP (Reference image read and preprocess) and For Test image read and preprocessing(TI_RPP) time taken will be around 152msec. In individual type defect localization, the inspection process will be carried out separately for detecting track cut, track short and pad damage and marking of individual defects with different colors. Total time taken is equal to the sum of time taken for an individual process. It is ranging from 1674msec to 1714msec (1.674 to 1.714 seconds) depending on the total number of defects present in the board and size of individual defects as shown in Table IV. In this method, it is possible to differentiate between the different types of defects because individual defects are marked by different color as shown in Fig 5(b).

In combined defect localization, defects are identified separately for a track cut, track short and pad damage. A single image is obtained by adding all the identified defects. Blobs of all defects are obtained in a single step and all defects are marked by the same color. Time taken for the complete process will be in the range of 670.119msec to 709.339msec depending on the total number of defects present in the board and size of individual defects as shown in Table V. Time taken by this method is almost three times lesser than that of individual type defect localization. Since all the identified defects are marked by the same color, It is not possible to differentiate between the different types of defects as shown in Fig 5(c).

Table -III : Location / Coordinates of Defects

Board Number	Nature-Number of Defects	Type of Defect	Cx	cy	size (r)	Marking coordinates			
						y1= (cy-r)	x1= (cx-r)	y2= (cy+r)	x2= (cx+r)

1	SD-1	Track cut	36	411	1.414	409	34	413	38
2	MSD-2	Track cuts	64	447	2.262	444	61	450	67
			25	339	2.262	336	22	342	28
3	MSD-3	Track cuts	279	231	2.262	228	276	234	282
			250	383	2.262	380	247	386	253
			171	368	2.262	365	168	371	174
4	MSD-4	Track cuts	385	68	2.262	65	382	71	388
			362	128	2.262	125	359	131	365
			62	251	2.262	248	59	254	66
			36	411	2.262	408	33	414	39
5	SD -1	Track short	133	295	9.264	285	123	305	143
6	MSD -2	Track shorts	155	359	3.624	355	151	363	159
			371	312	3.264	308	367	316	374
7	MSD -3	Track shorts	158	363	3.264	359	154	367	162
			116	250	3.264	246	112	254	120
			370	288	3.264	284	366	292	374
8	MSD -4	Track shorts	369	320	5.792	316	363	326	375
			351	89	5.792	83	345	95	357
			154	359	3.264	355	150	363	158
			92	446	5.792	440	86	452	98
9	SD - 1	Pad Damage	146	439	3.624	435	142	444	150
10	MSD -2	Pad Damage	205	398	3.624	394	201	402	209
			182	94	2.262	91	179	97	185
11	MSD -3	Pad Damage	143	482	3.624	478	139	486	147
			205	398	3.624	394	201	402	209
			182	94	2.262	91	179	97	185
12	MSD -4	Pad Damage	143	482	3.624	478	139	486	147
			205	398	3.624	394	201	402	209
			182	94	2.262	91	179	97	185
			67	128	2.262	125	64	131	70
13	MDD -2	Track cut-1	25	336	2.262	333	22	339	28
		Track short-1	371	225	5.792	219	365	231	377
14	MDD-3	Track shorts-2	155	359	3.624	355	151	363	159
			371	312	3.624	308	367	316	375
		Track cut-1	54	347	2.262	344	51	350	57
15	MDD-4	Track cuts-3	503	244	2.262	241	500	247	506
			422	333	2.262	330	419	336	425
			352	273	2.262	270	349	276	355
		Pad Damage-1	146	439	3.624	435	142	443	150

Table IV: Timing Analysis of individual type defect localization

Board No.	Nature -Number of Defects	Type of Defect	RI_RPP	TI_RPP	Time in milli seconds						
					Track cut inspection		Track short inspection		Pad damage inspection		Total
					FD	BD+ MKG	FD	BD+ MKG	FD	BD+ MKG	
1	SD -1	Track cut	320.27	151.59	1.002	511.3	0.998	504.2	1.001	504.2	1995
2	MSD - 2	Track cuts	-	151.59	1.002	519.8	0.998	504.2	1.001	504.2	1683
3	MSD -3	Track cuts	-	151.59	1.002	527.7	0.998	504.2	1.001	504.2	1691
4	MSD -4	Track cuts	-	151.59	1.002	535.6	0.998	504.2	1.001	504.2	1699
5	SD -1	Track short	-	151.59	1.002	504.2	0.998	518.3	1.001	504.2	1681
6	MSD -2	Track shorts	-	151.59	1.002	504.2	0.998	521.0	1.001	504.2	1684
7	MSD -3	Track shorts	-	151.59	1.002	504.2	0.998	529.5	1.001	504.2	1692
8	MSD -4	Track shorts	-	151.59	1.002	504.2	0.998	543.1	1.001	504.2	1706
9	SD - 1	Pad Damage	-	151.59	1.002	504.2	0.998	504.2	1.001	512.5	1675
10	MSD -2	Pad Damage	-	151.59	1.002	504.2	0.998	504.2	1.001	520.4	1683
11	MSD -3	Pad Damage	-	151.59	1.002	504.2	0.998	504.2	1.001	528.9	1692
12	MSD -4	Pad Damage	-	151.59	1.002	504.2	0.998	504.2	1.001	536.8	1700
13	MDD -2	TC1+TS1	-	151.59	1.002	511.9	0.998	514.2	1.001	504.2	1685
14	MDD -3	TC1+TS2	-	151.59	1.002	511.9	0.998	520.4	1.001	504.2	1691
15	MDD -4	TC3+PD1	-	151.59	1.002	527.7	0.998	504.2	1.001	512.5	1699

* FD: Fault Detection,
* BD+MKG: Blob Detection and Marking

Table V: Timing Analysis of combined defect localization

Board Number	Nature -Number of Defects	Type of Defect	Time taken in milli seconds					
			RI_RPP	TI_RPP	FD+ADD	BD	MKG	Total

1	SD -1	Track cut	320.27	151.59	6.019	509.01	2.3	989.189
2	MSD - 2	Track cuts	-	151.59	6.019	514.09	5.8	677.499
3	MSD -3	Track cuts	-	151.59	6.019	519.12	8.7	685.429
4	MSD -4	Track cuts	-	151.59	6.019	524.20	11.6	693.409
5	SD -1	Track short	-	151.59	6.019	509.01	9.3	675.919
6	MSD -2	Track shorts	-	151.59	6.019	514.09	7.0	678.699
7	MSD -3	Track shorts	-	151.59	6.019	519.12	10.5	687.229
8	MSD -4	Track shorts	-	151.59	6.019	524.20	19.1	700.909
9	SD - 1	Pad Damage	-	151.59	6.019	509.01	3.5	670.119
10	MSD -2	Pad Damage	-	151.59	6.019	514.09	6.4	678.099
11	MSD -3	Pad Damage	-	151.59	6.019	519.12	9.9	686.629
12	MSD -4	Pad Damage	-	151.59	6.019	524.20	12.8	694.609
13	MDD -2	TC1+TS1	-	151.59	6.019	514.09	8.1	679.799
14	MDD -3	TC1+TS2	-	151.59	6.019	519.12	9.9	686.629
15	MDD -4	TC3+PD1	-	151.59	6.019	524.20	12.2	694.009

The time taken by the individual type defect localization and combined defect localization for inspecting the boards containing a single defect with various size are tabulated as shown in Table VI.

Table VI: Timing Analysis for single defect with varying radii

Sl. No.	Radii of defect	Time taken in msec	
		Individual type defect localization	Combined defect localization
1	1.414	1674	668.919
2	2.262	1675	669.519
3	3.624	1676	670.119
4	5.792	1677	671.819
5	9.264	1681	675.919

Table VII: Timing Analysis of Inspection process with variation in number of defects

Sl. No.	Nature _Number of Defects	Time taken in msec	
		Individual type defect localization	Combined defect localization
1	SD_1	1675	669.512
2	MSD_2	1683	677.499
3	MDD_2	1685	679.799
4	MSD_3	1691	685.429
5	MDD_3	1691	687.227
6	MSD_4	1699	693.409
7	MDD_4	1699	694.009

As the size of defect increases time taken for the inspection of the board is also increases for both the types of defect localization. it can also be noticed that Individual type Defect Localization takes more time for the inspection of boards containing a single defect with various size compared to Combined Defect Localization. Time taken by Individual type defect localization and combined defect localization for inspecting the boards with Single Defect(SD), Multiple Similar Defects(MSD) and Multiple Different Defects(MDD) are tabulated as shown in Table VII. As the number of defects increases, time taken for the inspection of the board also increases for both the type of localization. it can be noticed that Individual type defect localization takes more time for the inspection of boards with the various number of defects compared to combined defect localization.

Most of the researchers worked on artificial PCB image (which includes the patterns of through-hole, surface mount, and Printed wiring board pattern), PCB laminate image and PCB layout image. Ibrahim used 400x400 Computer generated Artificial PCB image pattern which includes only 4 tracks, 6 SMT pads and 13 Through-hole pads[10]. Syed Abdul Rahman used 1kx1k PCB laminate image which includes only 7tracks, 10 SMT and 10 Through-hole pads[18]. Both the authors T.J. Mateo Sanguino and Ismail Ibrahim used simulated PCB Image which includes around 18 tracks and 30 holes[19],[20]. Wen-Yen Wu used 256 X 240 Computer generated Real PCB Pattern which includes only 6 tracks and 15 holes[9]. The proposed method used the real PCB board which are being used in particular products /Systems. Experimentation is conducted on 100 boards of two sets. All the boards of the first set contain 108 through-hole pads, 64 SMT pads, and 75 tracks. The second set of the board contains 105 through-hole pad, 66 tracks, and no SMT pads since this board design includes only through-hole components. Table VIII shows the comparison of nature of PCB image and inspection process time taken by the proposed system with that of other methods proposed by the various author. From this comparison, It can be noticed that the proposed method takes less inspection time compared to all other previous method even though the input boards are more complex and large size compared to the boards used by other methods. Since the experimentation is carried out on natural PCB and identified the defects along with location, the Proposed method can be directly used at the final inspection line of Bare Board PCB manufacturing industry. At the time of experimentation, totally 100 boards are inspected. Among 100 boards, 96 boards are inspected correctly and remaining 4 boards are not correctly inspected as the input images are scale downed. Table IX shows the details of detection and recognition rate using different scaling factor for these 4 incorrectly inspected boards. For the test PCB board TCSP311 having 3 track cuts,1 track short and 1 pad damage, the proposed method detects and recognize only 4 defects out of 5 defects if PCB board scaled down to 1024x1024 and 512x512 is used as input but it detects and recognizes all 5 defects for both 2048x2048 scaled-down and full-scale PCB image.

The boards TC12 and TS1 are correctly inspected only for full scale and 2048x2048 scaled-down input and the board PD_TH1 is correctly inspected only for a full-scale image. This missing of localization happens only when the radii of the defect are less than or equal to 1 or the size

Table VIII : Comparison of the proposed method with various other method

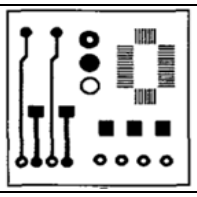
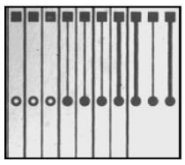
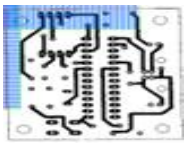
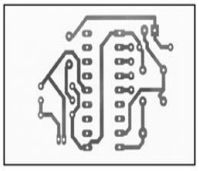
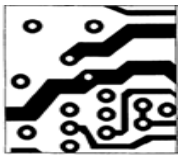
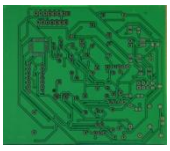
Sl. No.	Author	Size of the Image	Type of the PCB	PCB Image	Inspection Time in sec
1	Z. Ibrabim [10]	400 x 400	Computer generated Artificial PCB image pattern which includes 4 track, 6 SMT pads and 13 Through hole pads		4.686
2	Syed Abdul Rahman [18]	1k x 1k	Gray scale PCB laminate image		1.852
3	T.J. Mateo Sanguino [19]	1188 x1798	Simulated Real PCB Layout		1.668
4	Ismail Ibrahim [20]	1580×917	Simulated Real PCB Layout		28.78
5	Wen-Yen Wu,[9]	256 X 240	Computer generated Real PCB Pattern		15.68
6	Proposed System	4177x3681 (90mmx90mm)	Real Double sided PCB Board image		0.709 For combined defect localization 1.714 For Individual type of defect localization

Table IX: Details of incorrectly inspected board with different scaling factor

Name of the Test Board	Number of defects	Scaled down to 512x512		Scaled down to 1024x1024		Scaled down to 2048x2048		Full Scale Image	
		Detection No.(rate)	Recognition No,(rate)	Detection No.(rate)	Recognition No,(rate)	Detection No.(rate)	Recognition No,(rate)	Detection No.(rate)	Recognition No,(rate)
TCSP311	5	4(80%)	4(80%)	4(80%)	4(80%)	5(100%)	5(100%)	5(100%)	5(100%)
TC12	2	0(0%)	0(0%)	2(100%)	0(0%)	2(100%)	2(100%)	2(100%)	2(100%)
PD_TH1	1	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	1(100%)	1(100%)
TS1	1	1(100%)	0(0%)	1(100%)	0(0%)	1(100%)	1(100%)	1(100%)	1(100%)

of the defect is less than 3x3 pixels. From the overall experimentation, it can be noticed that full-scale image results in 100% detection and recognition, 2048x2048 scaled-down input results in 99% detection and recognition, 1024x1024 scaled-down input results in 98% detection and 96% recognition and 512x512 scaled-down input results in 97% detection and 96% recognition of the defects as shown in Table X . Automatic visual inspection (AVI) machine presently used in large scale PCB industries will take around 2 seconds to inspect the board of size 100mmx100mm. From the output of AVI machine, It is not possible to distinguish between the types of the defect. The proposed method of Individual type defect localization takes around 1.7 seconds to inspect the board of size 90mmx80mm. Here It is possible to distinguish between the types of the defect. The proposed method of Combined defect localization takes around 0.7 seconds to inspect the board of size 90mmx80mm. Here It is not possible to distinguish between the types of the defect.

V. CONCLUSION

In this paper real Bare PCB images are considered and mainly concentrates on the detection and Localization of defects which are results in major scrap in PCB manufacturing industries. The core concept of the proposed method is to extract the R band, B band, and grayscale image of RGB reference and test bare board PCB.

Track Short, Pad Damage and Track cut defects are identified using B band, R band, and grayscale images respectively. Localization of individual types of defects is obtained separately using Difference of Gaussian method and marked by different colors so that anyone can easily differentiate the type of defect. Localization can also be performed on the combined defects followed by marking with a similar color. In this case, it is not possible to differentiate the types of defect.

Table X:Inspection rate and time for different scaling factor

Input PCB Image	Detection Rate in %	Recognition Rate in %	Inspection time	
			Individual type defect localization	Combined defect localization
Full Scale	100	100	1.6minutes	32 sec
Scale downed to 2048x2048	99	99	24 sec	8 sec
Scale downed to 1024x1024	98	96	6.2 sec	2.2 sec
Scale downed to 512x512	97	96	1.7sec	0.7 sec

The proposed method is especially well suited for the inspection of the defects related to tracks and Pads of Real bare board PCB which are results in 67% of the total scrap. It takes less time and it can be implemented at low cost. Small scale industries can use this system at final inspection line of testing. It is possible to improve further by using parallel computation for processing the individual type of defect detection and localization which intern results in a faster and accurate inspection.

ACKNOWLEDGEMENTS

The authors wish to extend, their gratitude and appreciation to Mr. Nagendra Rao, Managing Director, DMS Technologies Pvt. Ltd., Mysore for his total support in this research by providing sufficient information about the most commonly occurred defects along with scrap analysis and sample bare board PCBs for it to be carried out. The authors also wish to extend their gratitude to Mr. S.Chiranjeevi, DGM (PCB&F), ITI, Bangalore and Mr. Amulya Mohapatra, Member Technical, Indian Printed Circuit Association, Bangalore for their technical input to carry out this research. Finally, Authors also appreciate the support of Maharaja Research Foundation, Mysore.

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