Modified Keeper Controlled Domino Circuit for Low Power High Performance Wide Fan in OR Gates

Manish Tiwari, Vijayshri Chaurasia, Bhavana P. Shrivastava, Laxmi Kumre

Abstract: A novel modified keeper technique has been proposed in this paper for domino logic circuits implemented as wide fan in OR gate. Few circuit parameters as capacitivie loading and delay are major concerns for OR gates in deeper technology nodes. This design focuses on a comparator block with modified dual keeperto maintain the output logic state. Additionally it comprises of a delay loop to limit the contention current. The proposed design reduces the input capacitive loading and total power consumption by the circuit, while keeping the speed of operation same. It was compared with latest domino circuit techniques and the proposed design MKCD has achieved a reduction of 41% in power consumption in 64 bit configuration as compared to conventional domino circuit SFLD. Average noise immunity has also increased by more than twice as compared to SFLD. The simulations were performed using 90nm PTM low power models.

Keywords : Dynamic logic circuits, OR gate domino, Modified keeper, Low power digital VLSI design.

I. INTRODUCTION

Dynamic logic circuits have represented the fast switching styles in industry and has been implemented in many gates, processors, memory circuits etc. The primary part of dynamic circuit involves clock driven transistor operation and the logic does not need a permanent latch to hold its output. Such factors allow it to operate at low power consumption as well as high speed [1-3]. Many of the applications that are of primary importance to communication and data transfer services, these can be based at logic gates designed by dynamic circuits. The futuristic systems demand more versatility in terms of battery usage and performance, and dynamic circuits reduce the power concumption of circuit efficiently while making it easy to use with interrupted power supplies aka that have lot of gaps between usage [4, 5]. Major applications of dynamic logic circuits are in microprocessor lines, MUX, etc.

With latest trends in nanometer scale CMOS technologies, the leakage current issues have grown along with other scaling dependent parameters. Such a trend can be favored only by technologies which have a tendency to reduce power leakage in any circuit design and dynamic logic offers a reliable solution because of the usage of clocked circuits as well as the scope for novel circuit designs in this area [6, 7]. Even the issues like reliability of output and excessive impedance related leakage can be resolved by using dynamic logic gates.

While dynamic circuit offers lot of advantages, realistic designs are needed in this area so as to cope up with the 4 major issues of dynamic circuits notably charge sharing and charge leakage [8-10]. Other issues are related to the clock synchornization and delay management [11]. As the technology nodes are miniaturized, better feedback techniques and higher stability of the circuits is demanded by the designers. This is to allow smooth operation of a circuit under variable process conditions. And these techniques should also have a reduced power consumption so that we can incorporate new domino designs for [12] and other logic circuits. Since every technique is designed based on trade offs and those trade offs in turn depend on various performance parameters of the circuit, below are the most important parameters we need to focus for a circuit as noise tolerance, gross performance of the circuit and power consumption.

A. Noise Tolerance

Many different methods are available to calculate the noise tolerance of a circuit but none of them give as complete picture as the noise tolerance ratio. It is because a circuit can have multiple noise source so if technology is changed, the noise tolerance parameter might show the same effect, however noise is much reduced in this situation. And vice versa too, if after changing circuit technology node or circuit design, the noise parameter shows no change but there can be changes in the tolerance of circuit. In order to judge the actual performance of the circuit, it is always advisable to use the output to input ratio as provided in (1). It is an important aspect of circuit design, but becomes far more crucial when circuit block interface and multiple supplies are used to design a particular logic gate.

* Correspondence Author

Manish Tiwari*, Electronics and Communication Department, MANIT Bhopal, M.P., India.

Vijayshri Chaurasia, Electronics and Communication department, MANIT Bhopal, M.P., India.

Bhavana P. Shrivastava, Electronics and Communication department, MANIT Bhopal, M.P., India.

Laxmi Kumre, Electronics and Communication department, MANIT Bhopal, M.P., India.

The straightforward approach to noise tolerance is being used here in order to find the stability of the circuit. This is generally called as unity gain failure criteria [13]. If any given circuit is operating at particular point and random noise is introduced, the change in output with respect to the input is recored to give the noise tolence of the circuit. If the condition is not satisfied, the noise performance is deemed low and the circuit will be seen as unstable circuit.

$$\left|\frac{dV_{out}}{dV_{in}}\right| > 1 \qquad (1)$$

Conventionally the approach used by most produce oriented industry tools is COT. However a better way to assess circuits is average noise immunity or ANI. Such will be presented in this paper, which has condition that if it is less than 1, it implies circuit is stable and also gives an idea about the degree of tolerance in the circuit.

B. Gross Performance of Circuit

Every deisgn focuses on improving the overall performance of the circuit. While 4 major parameters include area, noise tolerance, power consumption and speed of the circuit. Other parameters are also of importance as the reliability of the circuit, scalability of the circuit, tolerance to process variations and issues regarding cascading of the circuits. In order to verify the applicability of a design with respect to all these parameters, a novel performance parameter has been developed in this paper called Gross performance of circuit design or GPC. It is the conveyed figure of merit of any design as compared to others as given in (2).

$$GPC = \frac{ANI_n}{P_n \times t_n^2 \times A_n} \qquad (2)$$

This figure of merit allows for an uniased comparison between different domino circuit techniques, all kept at similar temperatures and other circuit initial points.

C. Power Consumption

The total power consumption of the circuit can be categorized in 3 separate parts as the dynamic power which is further divided as switching power and short circuit power, and static power or the leakage power consumption [14]. These components are given in (12) as follows.

$$P_{total} = P_{switching} + P_{short-circuit} + P_{leakage} \qquad (3)$$

$P_{switching}$ is the power consumption during the voltage switching and occurs due to the natural charging and discharging cycle for parasitic capacitive load. At deeper nodes, this becomes the major concern and is further explained in (4) as follows.

$$P_{switching} = \alpha C_{eff} V_{DD} V_{swing} f \qquad (4)$$

In the above equation, α stands for activity factor of switching. C_{eff} conveys the effective capacitance and f is for the frequency of switching. V_{DD} is the given supply voltage, while V_{swing} represents complete voltage swing as observed in the output terminal.

II. DOMINO CIRCUIT TECHNIQUES

Initially the domino variant of dynamic circuit was comprised of a standard pull down network alongside a pull up transistor. This configuration was noted as Standard Footed Domino [15]. It is represented in Fig. 1. domino techniques consider the 2 design strategies, either they focus on the feedback driven keeper path [16-19] or the evaluation pull up transistor block [20-25].

The conventional working of domino circuits include 2 modes as precharge and evaluate. In latest technologies, most gates are used in cascaded configuration in order to provide high through put and to be used in micro processor logic circuits too. For such purposes, Standard Footer Less Domino or SFLD was devised [16, 17] as given in Fig. 2.
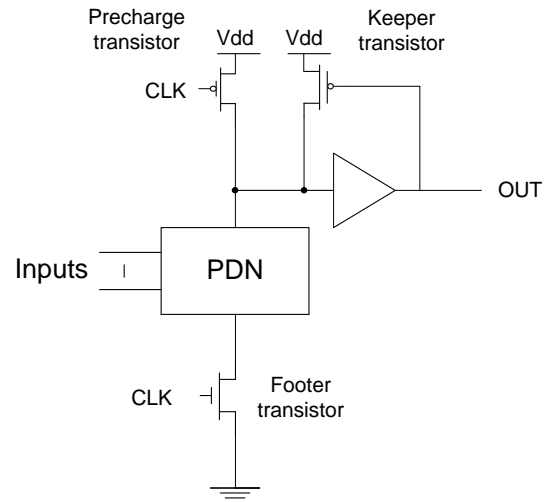

Fig. 1 Wide fan in Domino circuit as standard footed domino or SFD

Additionally, those systems that demand sophisticated loops and feedback, these are much more difficult to be managed with the conventional domino techniques due to the charge sharing issues. Novel designs are essential to cope up with such advanced circuitry and also for better battery optimizations.
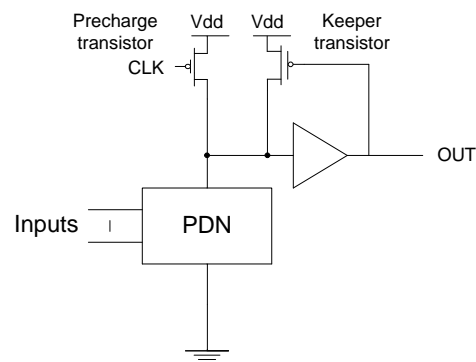

Fig. 2 Standard footerless or SFLD configuration for domino gate

Leakage current replica technique or LCR [22] is given in Fig. 3. It reflects the leakage current and mirrors it via the adjoining circuit. Such allows for low power consumption of the circuit by altering the switching of logic gates. However at higher number of inputs, this circuit stays at disadvantage due to the feedback solely driven by output. Therefore, in applications with high number of inputs, this logic style becomes less suitable unless it is modified for the output driven feedback mechanism.

This mirroring mechanism can be done in different ways, depending upon the final outcome of that circuit and the stringency of speed and power requirements. Given in [24], the current via reference block is being compared with the one from PUN. This is how a mirroring circuit reduces power consumption along with putting a high noise tolerance. Not only that, the control of circuit over logic output block is increased thereby leading to speedier operation and an increased robustness of the circuit. Such outcomes are highly desirable in a domino circuit.
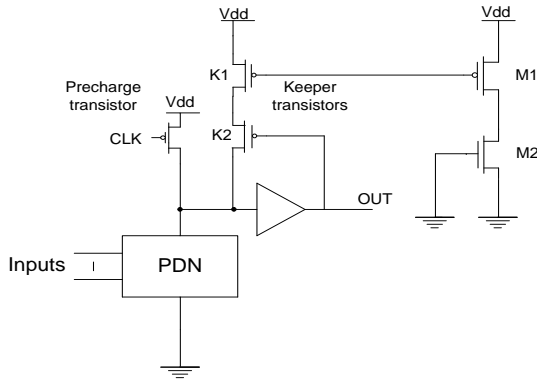

Fig. 3 Leakage current replicating design or LCR domino gate

Another popular way to mirror a circuit without leading the off putting block astray and while still maintaining the speed of operation, it is called controlled keeper current by comparison domino circuit or CKCCD [23]. It is represented in Fig 4(a) and Fig. 4(b). While this technique also has improved control, it incurs heavy input impedance and therefore requires a better strategy to reduce power consumption.
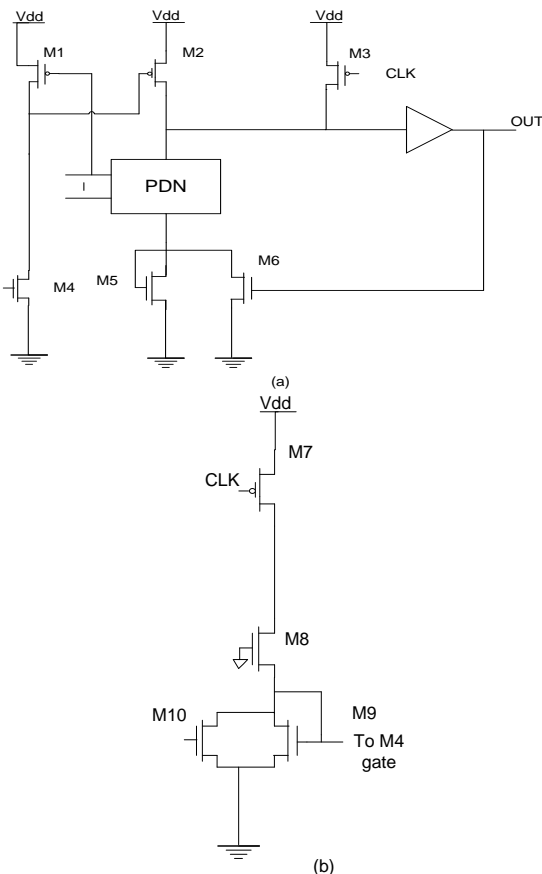

Fig. 4 (a) Controlled keeper current comparison domino or CKCCD main block (b) CKCCD reference block

Furthermore, diode partitioning technique or DPD [24] has been formulated to work efficiently for wide fan in gates. It allows reduced power consumption via better management of input capacitance. The typical diode or modified diode, both allow the speedier operation of the circuit along with reducing the power consumption considerably. However this incurs a heavy debt on area if we are to use keeper mechanism to shut down the circuit when not in use, and also other keeper defined strategies fall short of application here as the trade off for power fails.

Current comparison domino or CCD [25] is a highly favorable technique when it comes to mirroring mechanism along with a heavy reduction in contention current. It also incurs heavy debt in area, but most importantly it requires precise comparison and the process variations have high impact on CCD which is why it is not reliable for an industry standard technique. Mimor process variation sa re capable of mismatch the circuit and contention current will start to increase along with power losses.

III. PROPOSED DOMINO CIRCUIT

The proposed circuit consists of a single stage difference amplifier based comparator. And it was followed by a modified keeper that incurs a delay loop in order to reduce contention current. The input logic blocki is shown in Fig. 5 and the output logic block is shown in Fig. 6. The sizing consideration for all transistors were done by assessing the power losses incurred, speed of the circuit and the keeper ratio.

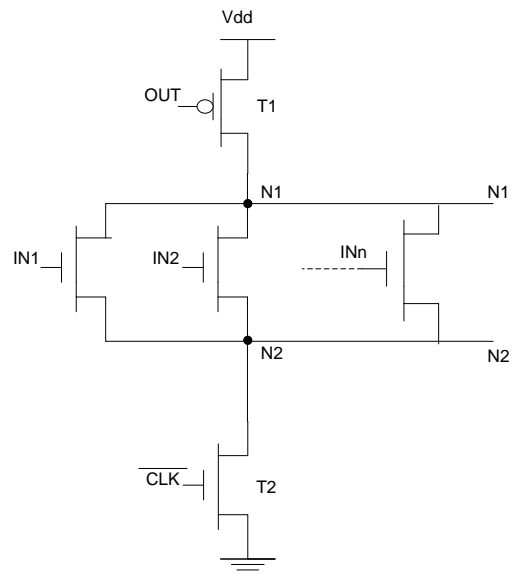**Fig. 5 OR gate design by MKCD Domino circuit input block**

In order to set up a base criteria to assess and evaluate the circuit, the keeper ratio has been introduced in this section in (5) and it has been used to formulate the design strategy needed for this circuit. Charge sharing and charge leakage were the necessary components to be avoided and in order to do so, the keeper size has to be kept at optimum level.

$$K = \frac{\mu_P (\frac{W}{L})_{Keeper-transistor}}{\mu_n (\frac{W}{L})_{Evaluation-network}} \quad (5)$$

This equation represents the width and lenth of the transistor respectively as W and L. Mobility of holes and electrons are represented respectively by μ_P and μ_n. The inference drawn from such arrangement is that, as we move to higher keeper ratio, the noise related performance of the circuit increases with it [26-30]. However it incurs additional delay. And if delay is to be reduced, noise performance will get degraded. Therefore new techniques are needed to overcome the mirroring issues as well as the management of optimal keeper ratio via transistor sizing constraints.
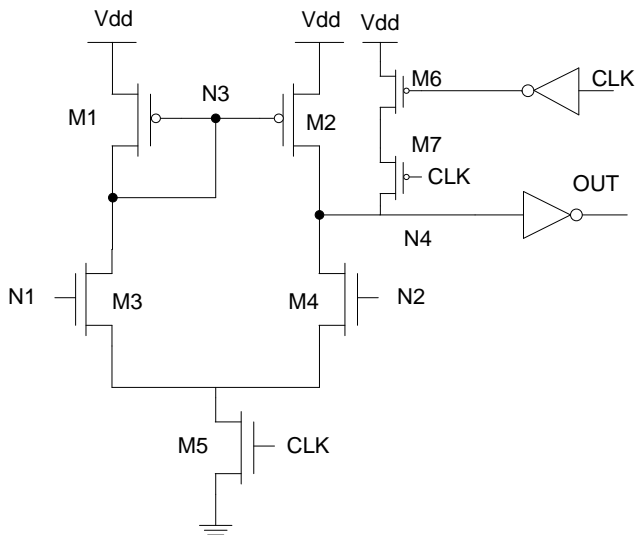

Fig. 6 OR gate design by MKCD domino circuit output block

The proposed design is modified keeper controlled domino circuit or MKCD.The primary obkective is to improve the noise tolerance of the circuit while keeping the same speed of operation. Additionally this circuit also achieves a reduced power consumption. The complete circuit will be discussed in 2 parts as the input and output logic circuit block.

In the precharge phase, capacitance turns to high and output goes in redundant low state, all the while clock is low at 0. The inputs are are also low in this state and N4 stays high. Transistor M7 is being used here to precharge the circuit and it ultimately reduces the output voltage to 0.

In the evaluation phase, clock is turned high and there are 2 possible input scenarios as either all or any is high, or else all are low. This leads to 2 different states at the output of domino OR gate. Here M6 is turned off. T1 and T2 will follow the reverse points aka T1 is On and T2 is off. N5 will be turned high in this phase. And lastly N4 will gain voltage before this phase and enter o state or 1 state depending upon the input combinations.

The delay element works in favor of reducing the contention current by cutting off the power supply to keeper transistor, when the circuit in in evaluation phase. Such an effort maintains a steep curve at output for the voltage rise and reduces power consumption efficiently.

IV. RESULTS AND DISCUSSION

The entire circuit has been compared on performance metric similar ground, such that unbiased comparison can be discussed. All simulations have been performed using 90nm PTM low power models. And the temperature used for comparison is 110 ℃ so as to assess the operation on higher than usual temperatures which is 90-100 ℃ mostly. Voltage supply is kept at 1 volts. Below is the comparison of proposed design MKCD with other domino circuit designs for average noise immunity metric, as given in table 1. The proposed design has acquired a higher noise tolerance than conventional SFLD as well as latest designs like CCD, CKCCD etc. At 64 bit configuration, it provides more than twice the noise tolerace as provided by the conventional SFLD circuit thereby proving its efficacy in terms of noise metric.

Table 1: Average Noise Immunity metric compared for 6 different designs at same delay used in 4 different input configurations as 8 bit, 16 bit, 32 bit and 64 bits.

Fan-in		SFLD	LCR	DPD	CKCCD	CCD	MKCD Proposed
8	ANI	0.45	0.37	0.48	0.66	0.68	*0.70*
16	ANI	0.39	0.32	0.46	0.63	0.66	*0.69*
32	ANI	0.34	0.29	0.45	0.57	0.61	*0.67*
64	ANI	0.29	0.25	0.44	0.54	0.54	*0.62*

The dynamic and static power consumption has been another area of major concern considering the increased number of transistors and area in these sophisticated circuits. At 8 and 16 bit configuration, MKCD was unable to provide the best output due to the extra delay transistors aligned in it as shown in table 2.

Table 2: Power consumption metric compared for 6 different designs at same delay used in 4 different input configurations as 8 bit, 16 bit, 32 bit and 64 bits.

Fan-in		SFLD	LCR	DPD	CKCCD	CCD	MKCD proposed
8	P_t	25.3	24.5	29	*20*	23	29.2
16	P_t	29.4	27.6	34.2	23.6	*22.3*	27
32	P_t	34.75	34	39.3	30	24.9	*23.8*
64	P_t	44	40	48	38	27.5	*25.6*

However due to the reduced input capacitance related losses and the feedback associated reduced voltage swing at the output node, the proposed design MKCD has achieved 31.5% and 41.8% reduced power consumption as compared to SFLD in 32 bit and 64 bit configuration respectively. And also has achieved 32.6% and little less than 7% reduction as compared to CKCCD and CCD respectively in 64 bit configuration.

Major parameters of the circuit are all compared below while being kept under same delay of 90ps. This is to ensure proper quality check of a design since they all incur different design induced delays.

GPC is the commo paramer to determine the combined efficacy of a domino circuit design. Below in table 3, 32 bit configuration is being used considering it is the most common one in current wide fan in gate circuits. GPC of proposed design is higher by 55% as compared to basic SFLD circuit. While the proposed design incurs some additional circuit area, it provides a higher noise tolerance of 0.67 that is more than twice the best domino design and is of utmost importance to real time communication circuits.

Table 3: All performance parameters compared for 6 different domino circuit designs at same delay working under 32 bit configuration.

	Total transistors	Area	Power	ANI	GPC
SFLD	*36*	*125*	34.75	0.34	1
LCR	39	133	34	0.29	0.67
DPD	84	291	39.3	0.45	0.93
CKCCD	44	151	30	0.57	0.83
CCD	48	238.5	24.9	0.61	1.2
MKCD	45	159	*23.8*	*0.67*	*1.55*

V. CONCLUSION AND FUTURE WORK

Current domino circuits involve the speedier operation of systems while providing easy design methods to reduce the contention current and leakage issues. However with deeper technology nodes, leakage issues will become much more prominent. Also with the lowering of voltage supply, even though it has reached a lowest mark and tradeoff situation has arisen where further lowering voltage supply will only lead to higher power consumption. Still with latest technologies, novel design strategies are needed to implement high performance circuits.

Domino circuits made from MKCD strategy provide the least power consumption alongside a high noise tolerance, at the expence of minor additional circuit area and this technique is capable of integrating with future techniques that work focused on deep technology nodes. The proposed design has reliably increased the performance of the circuit in lieu of process variations and technology node variations too. The proposed design has also proved to occupy same speed of operation while providing the reduction in dynamic power and has scope for future improvement in terms of the stand by issues, voltage scaling issues and the threshold voltage related leakage current management concerns. MKCD improves the performance parameters via reducing the voltage swing at the output of domino circuit. This voltage swing has been reduced efficiently as compared to latest domino circuit designs via using the single stage comparison technique.

The simulations of domino circuits were performed using 90nm PTM low power models. The proposed MKCD is applicable in designs that demand higher bit lines or data paths as in micro processor, battery optimizations and memories, as well as systems that need high fan in gate operations.

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AUTHORS PROFILE

Manish Tiwari received Bachelor of Engineering degree in Electronics and Instrumentation in 2008 and MTech from Nanotechnology at MANIT Bhopal, India. He has published research papers in international conferences and journals and has been trained in chip fabrication at IISc Bangalore.
Currently he is pursuing PhD research work in the area of low power dynamic logic circuits in Electronics and Communication department at MANIT Bhopal.

Vijayshri Chaurasia received Bachelor of Engineering degree in Electronics and Communication in 2005 and MTech in Digital Communication and PhD in Image Processing from MANIT Bhopal, India.
She has published more than 65 research papers in national and international journals and conferences, as author and co-author. She is a recipient of MP Young Scientist Award 2012 for electronics, communication and instrumentation. She is a member of technical bodies as IEEE, IETE and ISTE.
Currently she is working as Assistant Professor with MANIT Bhopal, India and is involved in research of low power electronics and biomedical image processing.

Bhavana Prakash Shrivatava received her Bachelor of Engineering degree in Electronics and Communication Engineering in 2003, M.Tech. in Digital Communication Systems in 2007 and PhD degree in the field of VLSI Design in 2014. She has 24 publications in various international conferences and journals.
Currently she is working as Assistant Professor in Electronics and Communication Engineering in MANIT, Bhopal. Her fields of interest are VLSI design and Communication Systems,circuit design and networking.

Laxmi Kumre received her Bachelor of Engineering degree in Electronics and Communication , M.Tech in Digital Communication and PhD in VLSI Design. She has published more than 20 research papers in international conferences and journals, and is a member of professional bodies IEEE and IETE. Sha has supervised project for model based design forimplementation in logic chip designing.
Currently she is posted as Assistant Professor in ECE department MANIT Bhopal. Her research areas include multi processor and mico architecture designs, distributed and parallel computing, optical communication and VLSI design.