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A New ALU Design using PNS-FCR: Static CMOS Logic for Microprocessors

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Abstract*: *Arithmetic Logic Unit (ALU) is the main component in the processors. Most important design consideration in integrated circuit is power. In all the components of ALU data path is the active one and it consumes more percent of power in the total power. In the modern microprocessors it is important to have power efficient data paths. To reduce the power consumption in microprocessors the ALU is designed using PNS-FCR static CMOS logic. In this paper static CMOS logic is used to reduce power consumption. Static technique does not need any clock. So it leads to less power consumption. For the implementation of the ALU with the PNS-FCR static logic mentor graphics tool is used. The power consumption of ALU is compared with and without using FCR. An 8-bit ALU is designed in mentor graphics with 130nm technology. The proposed design methodology gives less power consumption.

Key words*: *PNS-FCR, Static CMOS logic, ALU

I. INTRODUCTION

The transistor count on the chip is increasing continuously day by day. So the power consumption also became the major issue in the processors design and in many application. Power consumption [4] is the one of the component whichn plays crucial role in any the microprocessors design particularly targeting Low Power Embedded Systems. In the microprocessors the data paths that performs computing operation also consumes more power mainly in critical paths. The power efficient circuit means consuming less power. The CMOS technology which involves making/designing low power devices since few decades. CMOS has less power dissipation by Comparing with different logic families of CMOS. In the modern microprocessors, data paths [6] consumes more percent of total power consumption. So it is more important to achieve more efficient data paths that consumes less power consumption In order to get low power extra circuitry is used that gives less power consumption in microprocessors.

In this paper, a novel ALU is designed with PNS-FCR [1] static CMOS logic (n-type/p-type selection, flexible charge recycling), which gives high power efficiency in the data paths of microprocessors.

In this paper the following primary contributions are made.

1) Different logic styles are mentioned and the one that is used is described.
2) The PNS-FCR method is described which provides charge recycling path.
3) Various adder circuits are analyzed using static circuit techniques and suitable adder to be used in the ALU design.
4) Power analysis of ALU is provided and results are compared .

Different CMOS logic styles:

1) Static CMOS logic:
   Gives less static power consumption
2) Complementary Pass Transistor logic :
   Large power consumption
3) Transmission Gate logic:
   Lack driving capability
4) Dynamic logic:
   More power consumption because of high switching activity.

The work mainly concentrate on minimize the power consumption in microprocessors using CMOS logic(static).

II. CMOS LOGIC (STATIC)

Static CMOS logic [3] called as static because it doesn't depend on the stored charge for their operation. And it is called as complementary because it is constructed from p-type and n-type transistors complementary (dual) networks. The Static CMOS [7] logic is divided into (pull up network) PUN and (pull down network) PDN. PUN is made of p-type transistor and PDN is made of n-type transistor. In PUN, the output is connected to Vdd and to Vss through the PDN. For an n-inputs static CMOS logic uses 2n transistors during implementation. CMOS gates consumes power during the transitions. The figure 1 shows the CMOS logic with pull up and pull down network. Using PDN with PUN, the complete CMOS gate is constructed..

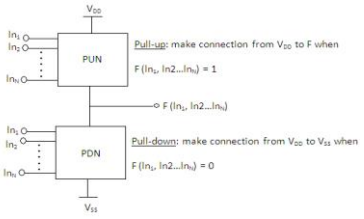

Fig.1. CMOS gate with PUN and PDN.

Static CMOS logic having following basic features:

- There is no Power dissipation of static
- Swing of Full rail to rail that gives noise margins
- Speed of static CMOS depends on transistor sizing
- More area is required

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- output impedance is low and the input impedance is high
- In between V_{DD} and GND there is no steady state path
- Delay depends on transistor resistance and load capacitance

III. PNS-FCR

A PNS algorithm (n-type/p-type selection) and a flexible charge recycling (FCR) design methods are proposed to achieve low power in data paths. PNS static CMOS logic [8] with the charge recycling path is proposed to reduce the power consumption,. In race free pipelines and power gates circuits charge recycling is used. There are so many charge recycling [2] [5] techniques are used previously. In this work the flexibility in charge recycling path which is optimized to two transistors only and it gives more efficient data paths. The two transistors are connected in such a way that the power consumption is decreased and they avoid the threshold voltage influence on the power.

The FCR cell is designed with two n-type transistors in series where one transistor gate is given to clkb and other transistor gate is shortened with source. The FCR cell can be inserted between two neighboring gates and between two independent gates. It creates charge recycle path between the gates. And it works like a switch. The figure 2 shows the adder cell with FCR cell.

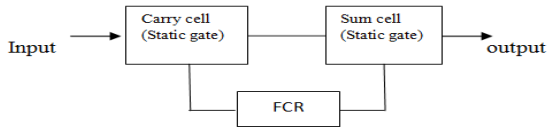

Fig.2. adder cell with FCR cell

The FCR cell occupies a very little portion in the area of the entire adder. The FCR to be considered for the reduction of power consumption and silicon area. The power consumption and speed are the most priority then FCR is preferred.. Flow diagram of PNS-FCR method shown in Figure 3.

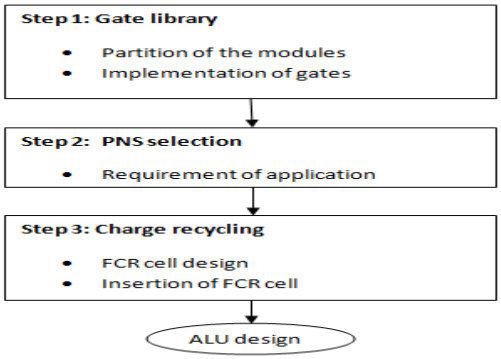

Fig.3. Proposed PNS-FCR method

The steps involved in the PNS-FCR static CMOS logic are described below and the flow diagram is shown in above figure. The steps are

1) First step is partition of the modules in the ALU. The gates in the modules are designed with static CMOS logic.

2) On the requirement of applications the gates are selected to design ALU.

3) The FCR cell is designed to provide charge recycle path in the critical data path. The FCR cell is inserted in between the neighboring gates or in the individual gates.

4) For more power efficient data paths the FCR cell may be inserted in non critical paths also.

IV. DESIGN OF STATIC CMOS ALU WITH FCR

Basically ALU is the main block in all the processors. ALU performs both logical and arithmetical operations, so called ALU (Arithmetic and Logic Unit). This circuit will perform logical operations such as AND, OR, XOR, NOT and SHIFT and arithmetical operations such as ADD and SUBTRACTOR. The critical paths in the ALU determines the delay of ALU. Figure 4 shows the block diagram of Arithmetic Logic Unit (ALU).

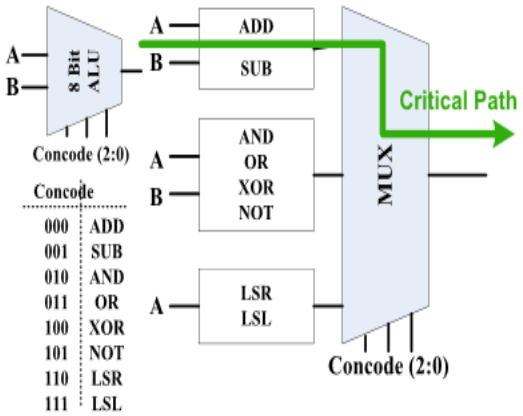

Fig.4. Arithmetic Logic Unit (ALU) block diagram

Basically in the ALU, the adder is slower compare with all other modules. That is the critical path in the ALU. There are so many types of adders present in which the ripple carry adder gives less power consumption than others.

In this paper the adder module is designed with ripple carry adder with FCR cell.The 8-bit ALU is designed and shown in Figure 8. The technology used to design ALU is 130nm technology.

Adder is present in the path so FCR cell is inserted in the module which gives less power consumption.

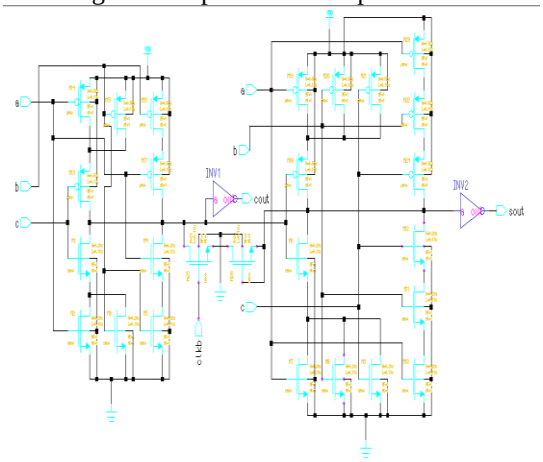

Fig.5 . Adder with FCR cell

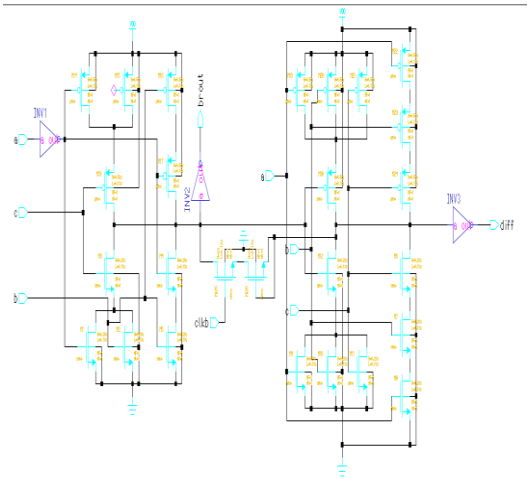

Fig.6. Subtractor with FCR cell

The design shown below is the 8-bit ALU with using the FCR cell. ALU consists of INVERTER, AND, OR, EXOR, ADDER, SUBTRACTOR, left shift and right shift modules for 8-bits.

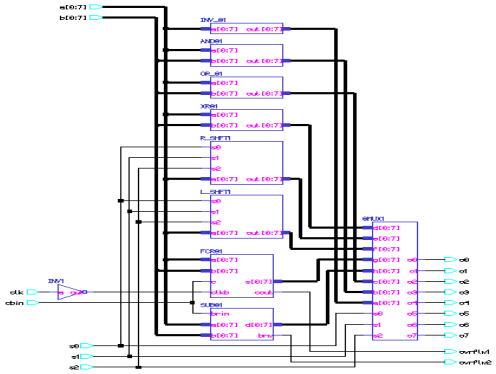

Fig .8.8-bit ALU with FCR

V. RESULTS

The schematic representation of 1-bit inverter which is designed with Static CMOS logic as well as outputs is shown in figure 9. For the 8-bits the inputs and outputs are given as bus like [0:7] shown in Fig 10.

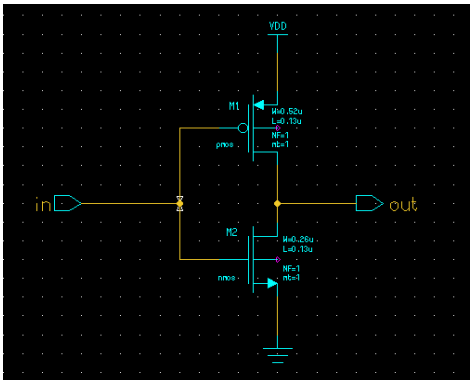

Fig .9. Schematic of inverter for 1-bit using CMOS logic

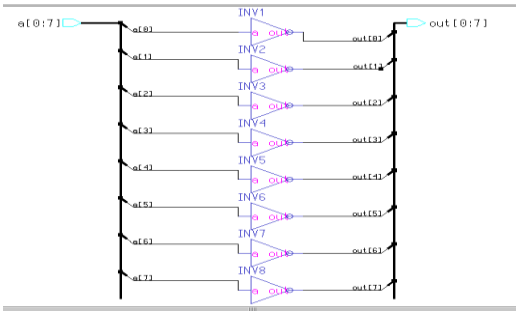

Fig.10. Schematic of inverter for 8-bits using CMOS Logic

The trancient analysis of inverter shown in Fig 11 and operation is observed where V(A) indicates input and V(out) indicates output of the inverter gate.

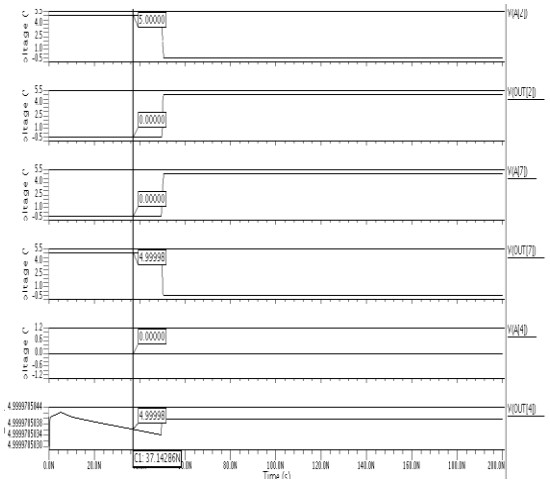

Fig.11. Transient analysis for inverter

The schematic representation of AND which is designed with Static CMOS logic as well as outputs is shown in figure 12. For the 8-bits the inputs and outputs are given as bus like [0:7]. Shown in fig 13. Fig 14 shows the Transient Analysis of AND gate.

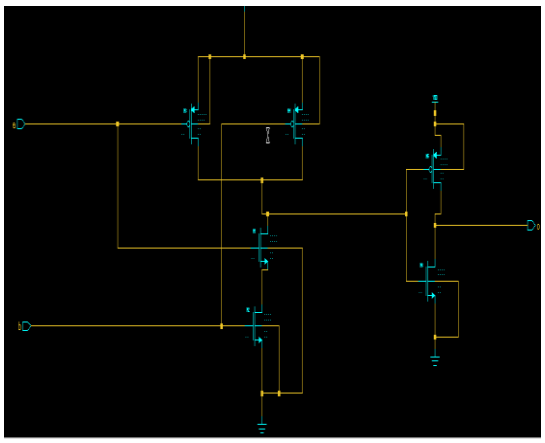

Fig.12. Schematic of AND for 1-bit using CMOS logic

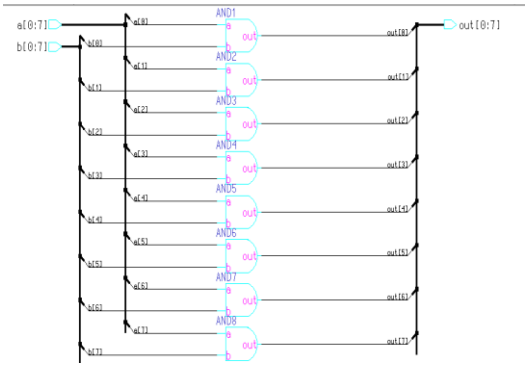

Fig.13. Schematic of AND for 8-bits using CMOS logic

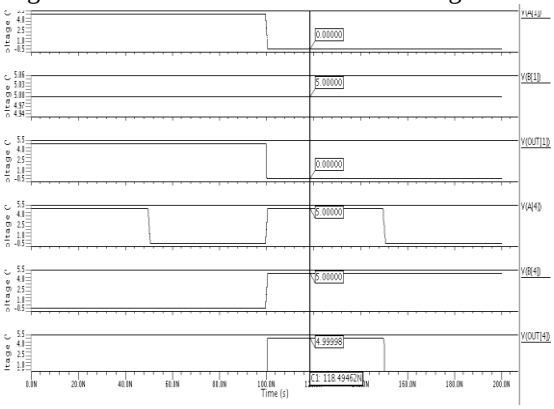

Fig.14. Transient analysis for AND logic

The schematic representation of OR which is designed with Static CMOS logic as well as outputs is shown in figure 15. For the 8-bits the inputs and outputs are given as bus like [0:7] shown in fig 16. Transient analysis of OR gate shown in fig 17.

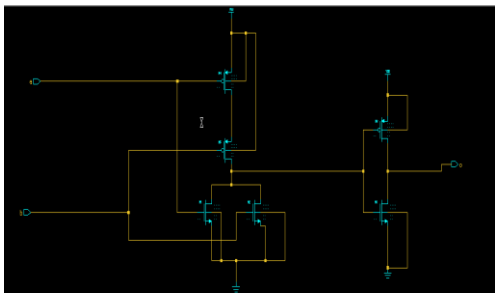

Fig.15. Schematic of OR for 1-bit using CMOS

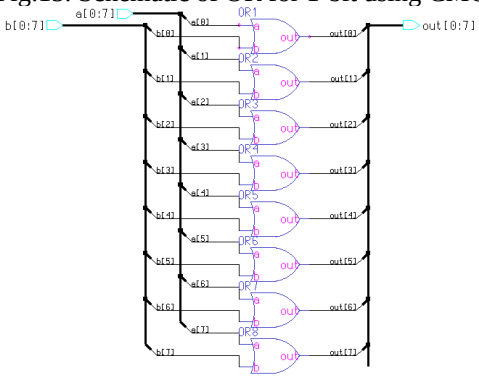

Fig.16. Schematic of OR for 8-bits using CMOS logic

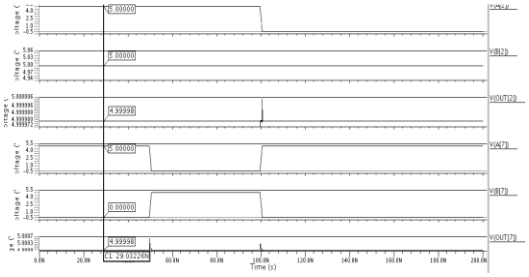

Fig.17. Transient analysis of OR logic

The schematic representation of EXOR which is designed with Static CMOS logic as well as outputs is shown in figure 18. For the 8-bits the inputs and outputs are given as bus like [0:7] show in 19. Transient analysis of EXOR gate shown in fig 20.

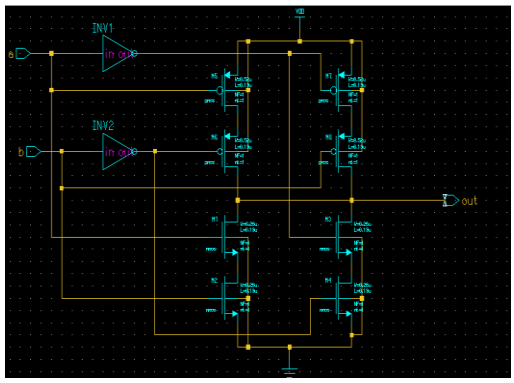

Fig.18. Schematic of EXOR for 1-bit using CMOS logic

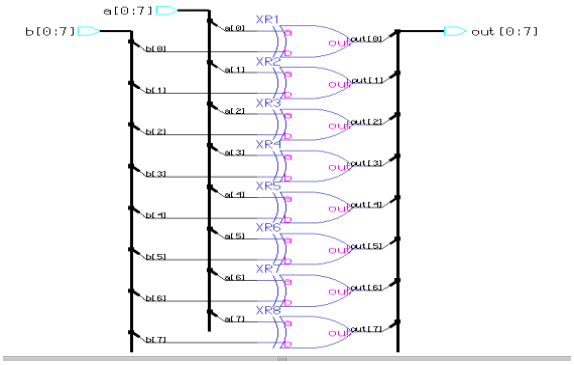

Fig.19. Schematic of EXOR for 8-bits using CMOS logic

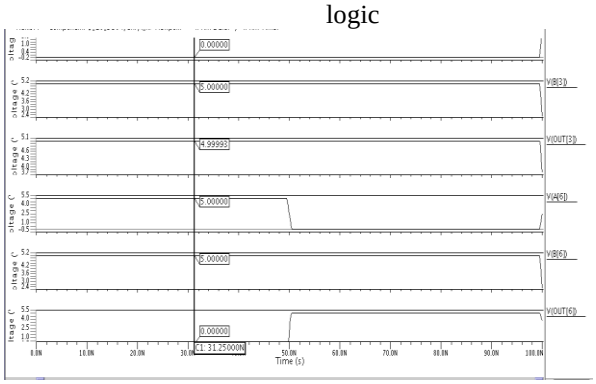

Fig.20. Transient analysis for EXOR logic

The schematic representation of LEFT SHIFT which is designed with Static CMOS logic as well as outputs is shown in figure 2. For the 8-bits the inputs and outputs are given as bus like [0:7] shown in fig 21. Trancient analysis of LEFT SHIFT circuit shown in fig 22.

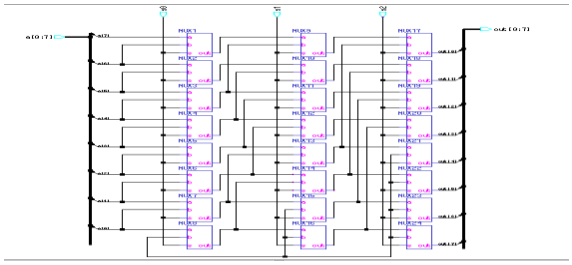

Fig.21. Schematic of Left shift for 8-bits

Based on the selection it will shift the input from 1 to 8 positions to the left side.

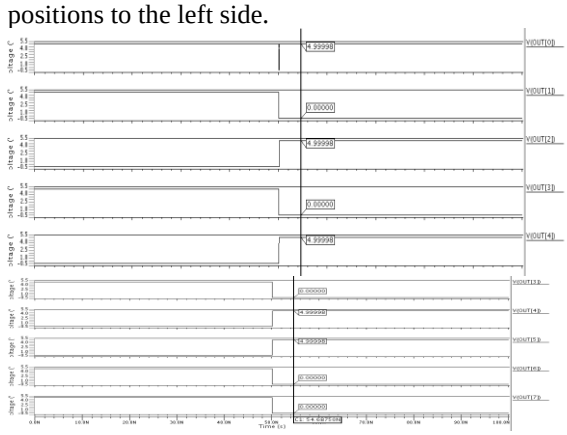

Fig.22. Transient analysis for Left Shift operation

The schematic representation of RIGHT SHIFT which is designed with Static CMOS logic as well as outputs is shown in figure 23. For the 8-bits the inputs and outputs are given as bus like [0:7] shown in fig 23.

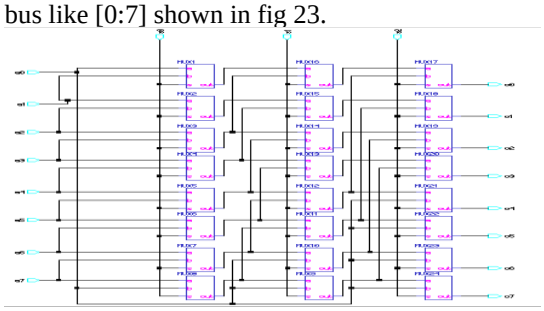

Fig.23. Schematic for Right Shift for 8-bits

Based on the selection it will shift the input from 1 to 8 positions to the right side.

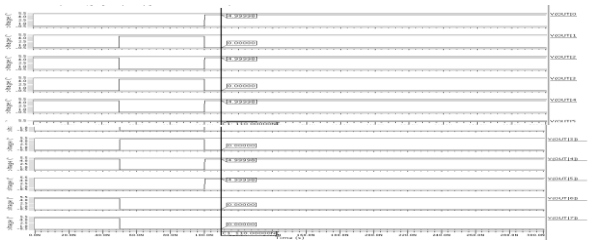

Fig.24. Transient analysis for Right Shift logic

The schematic representation of ADDER which is designed with Static CMOS logic as well as outputs is shown in figure 25 without FCR cell.

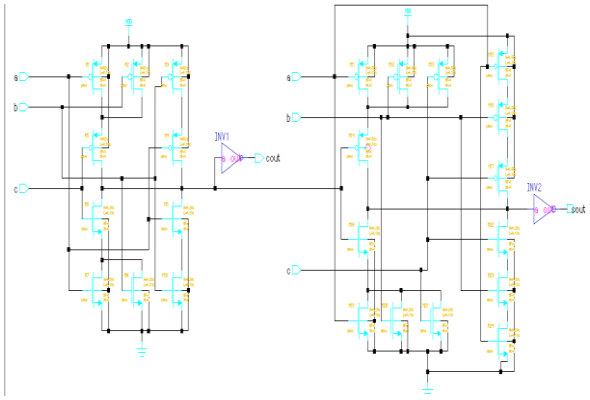

Fig.25.Schematic of full adder without FCR cell

The schematic representation of Ripple Carry Adder which is designed with Static CMOS logic as well as outputs is shown in figure 26 without FCR cell. For the 8-bits the inputs and outputs are given as bus like [0:7] shown in fig 27..

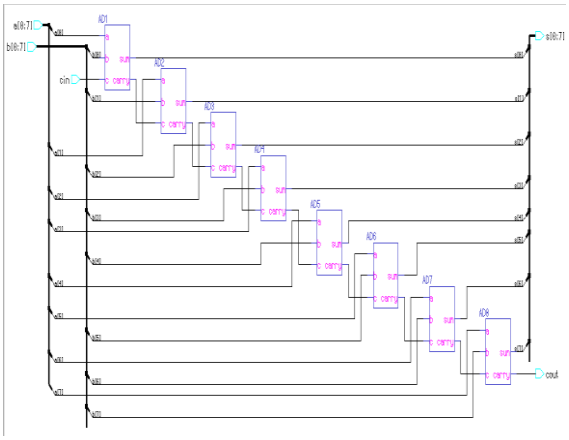

Fig.26. Schematic of ripple carry adder for 8-bits

Basically ripple carry adder gives less power consumption. The schematic representation of Ripple Carry Adder which is designed with Static CMOS logic as well as outputs is shown in figure 27 with FCR cell. For the 8-bits the inputs and outputs are given as bus like [0:7] shown in fig 27. The trancient analysis of ripple carry adder with FCR cell shown in fig 28.

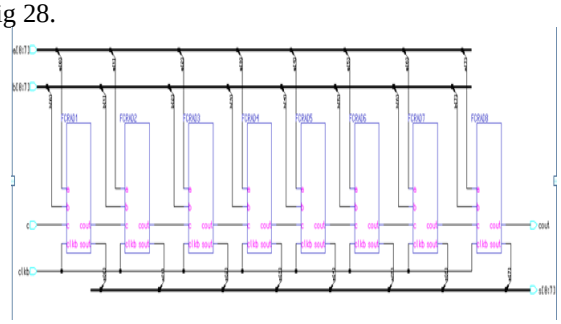

Fig.27. Schematic for ripple carry adder with FCR cell

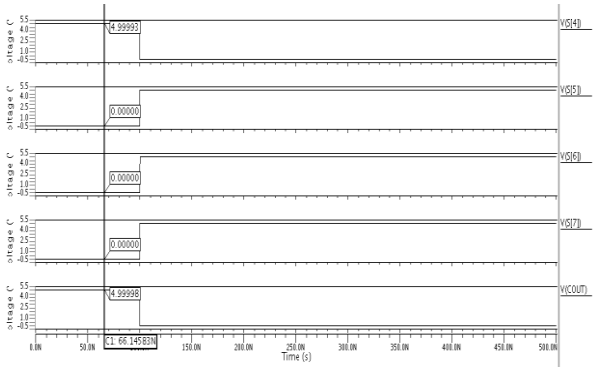

Fig.28. Transient analysis for ripple carry adder

The schematic representation of SUBTRACTOR which is designed with Static CMOS logic as well as outputs. without FCR cell. For the 8-bits the inputs and outputs are given as bus like [0:7] shown in fig 29.

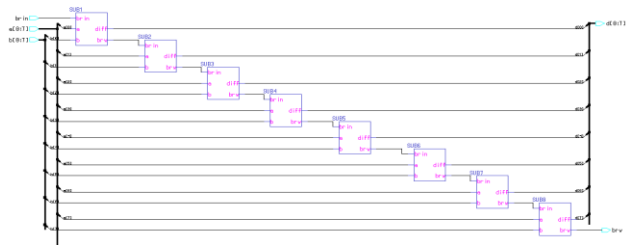

Fig 29: Schematic for subtractor for 8-bits without FCR cell

The schematic representation of SUBTRACTOR for 8-bits which is designed with Static CMOS logic as well as outputs is shown in figure 30 with FCR cell. Transient analysis of Subtractor with FCR cell shown in fig 31.

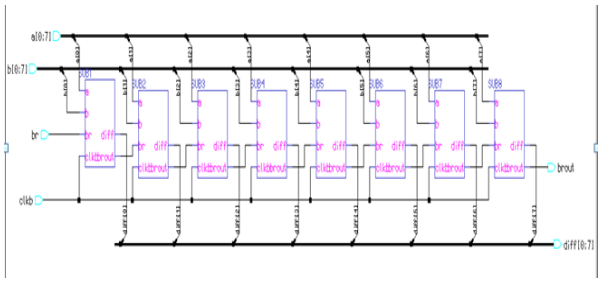

Fig.30. Schematic for subtractor with FCR cell for 8-bits

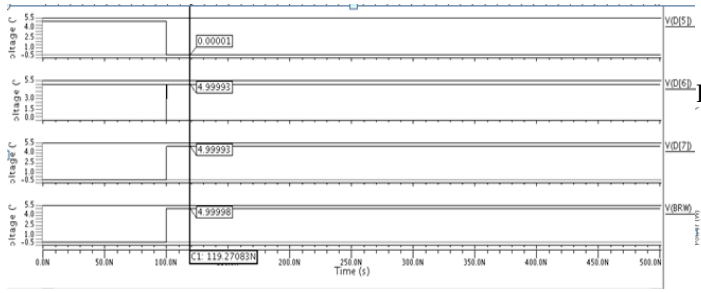

Fig.31. Transient analysis for subtractor with 8-bits

The schematic representation of 8x1 multiplexer for 8-bits which is designed with Static CMOS logic as well as outputs is shown in figure 32.

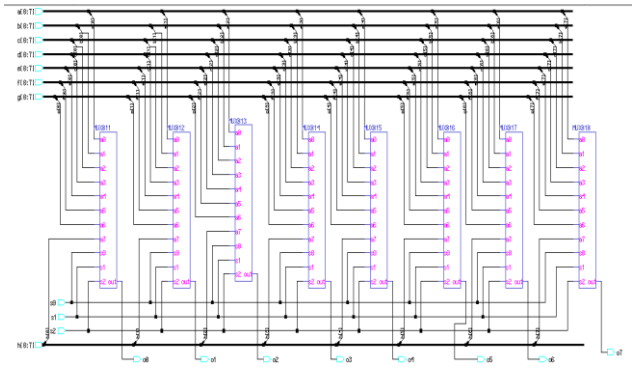

Fig.32. Schematic of 8-bit 8x1 multiplexer

Finally after completing the all modules cascode all the modules by 8x1 mux to design ALU. The schematic representation of ALU with and without FCR is shown in figure 33.and fig 8 shows the FCR cell.

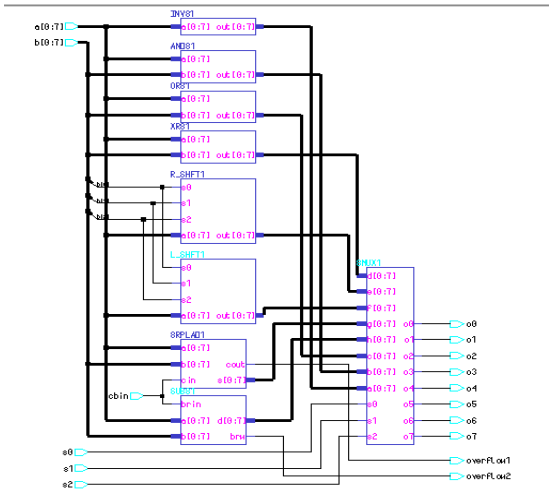

Fig.33. Schematic of 8-bit ALU without FCR cell

The power analysis for the ALU without and with using the FCR cell shown in figures 34 & 35 respectively.

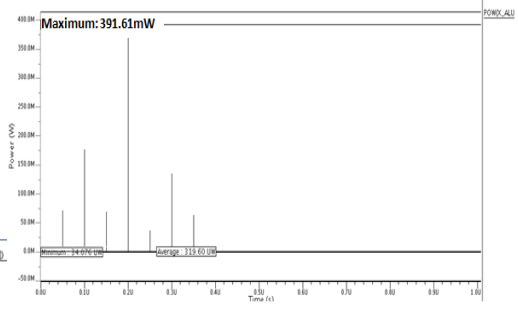

Fig.34. power analysis of 8-bit ALU without FCR

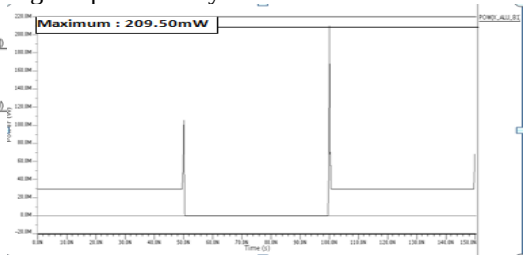

Fig.35. power analysis of 8-bit ALU with FCR cell

After implementation of all the modules in the ALU with FCR cell simulation of ALU is done that gives less power consumption. The area may be large but power consumption is reduced.

Table 1: Power Consumption of an 8-bit ALU, without and with FCR cell (Static Logic)

Operations	Power consumption (mW)	
	Without FCR	*With FCR*
ADD	64.861	8.9530
Subtract	68.530	9.7130
ALU	391.61	209.50

VI. CONCLUSION

An 8-bit ALU is designed using static CMOS logic which gives less power consumption. An efficient ALU in terms of power is designed with using the FCR cell. The power is compared for adder, subtractor and ALU without and with using the FCR cell. The power consumption of an ALU with FCR cell, the power saving can be 53% compared with ALU without FCR cell. The power consumption of ALU with FCR cell (Dynamic logic) [1] compared with Conventional ALU, power saving about 30%. This charge recycling method is also extended to different logic styles.

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