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A 5 Bit 600MS/S Asynchronous Digital Slope ADC with Modified Strong Arm Comparator

Nadendla Bindu Priya, Muralidharan Jayabhalan

Abstract—Strong arm comparator has some characteristics like it devours zero static power and yields rail to rail swing. It acquires a positive feedback allowed by two cross coupled pairs of comparators and results a low offset voltage in input differential stage. We modified a strong arm Comparator for high speed without relying on complex calibration Schemes. a 5-bit 600MS/s asynchronous digital slope analog to digital converter (ADS-ADC) with modified strong arm comparator designed in cadence virtuoso at 180nm CMOS technology. The design of SR-Latch using Pseudo NMOS NOR Gate optimizes the speed. Thus delay reduced in select signal generation block. Power dissipation is minimized with lesser transistor count in Strong arm comparator and SR-Latch with maximum sampling speed. The speed of the converter can be improved by resolution. The proposed circuit is 5-bit ADC containing a delay cell, Sample and hold, continuous time comparator, strong arm comparator, Pseudo NMOS SR-Latch and Multiplexer. This 5-bit ADC operates voltage at 1.8 volts and consumes an average power.

Keywords—Pseudo NMOS, strong arm comparator, asynchronous digital slope analog to digital converter (ADS-ADC)

I. INTRODUCTION

This paper modified a selection signal generation block at the architecture of asynchronous digital slope analog to digital converter by using modified strong arm comparator and ratioed logic. The ratioed logic is used in NOR gate SR-Latch. In SR-Latch we are replaced a Pseudo NMOS NOR Gate. We are modified the strong arm comparator and we can reduce the delay. The strong arm comparator reduces the amount of cells delayed and connects these outputs in a selections signal generation block to the inverters and inverter outputs to SR-Latch inputs. The pseudo NMOS is used to reduce the power. The ADC characteristics are to produce the rail to rail outputs and consume the zero static power. Compared to this (1) we can improved a sampling speed by using a modified strong arm comparator (2). In this ADC we are converting to the use of converters are pipeline ADC (3), (4). And Successive Approximation (SAR) ADC(5). The thermometer code is converted to binary code by the decoder. For code conversion we are used a 16-bit multiplexer based decoder (7),(8), that decoder is used for the reduction of propagation delay. Section II is the asynchronous digital slope ADC circuit designs section III is presents the simulation results section IV gives the conclusion.

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* Correspondence Author (s)
Nadendla Bindu Priya, E.C.E VFSTR Guntur, Andra Pradesh. nadendlabindu1996@gmail.com
Muralidharan Jayabhalan, E.C.E, Assoiate Professor VFST Guntur, Andra Pradesh muralidharanae@gmail.com

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II. ASYNCHRONOUS DIGITAL SLOPE ADC

In the architecture of asynchronous digital slope ADC the differential inputs are Vin+ and Vin-. the sampling clock is connected to the CLK signal. at the same time as sampling period the CLK is "1", the modified block compares to input signals and yields the outputs of SP and SN for multiplexers as shown below figure. Vin+>=Vin- the output of SP is High and C+ pursues OUTP C- pursues OUTN. when Vin+<=Vin- the output of SN is High C+ pursues OUTN and C- pursues OUTP as shown in fig 1.QN and QP are the output of delay cells, the output QN of delay cell 1 enabled from 1 to 0, where QP is 0 to 1. C0 is the capacitor array that is attached to the delay cell outputs.

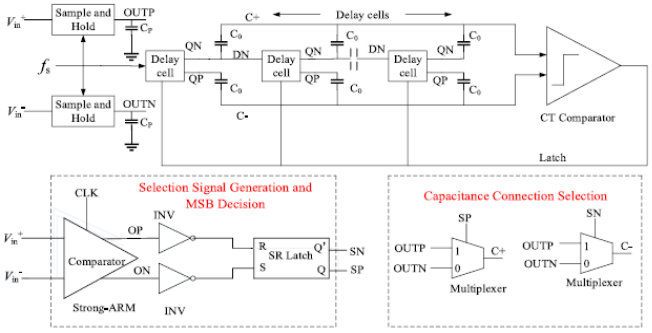

Fig 1: Symbolic representation of Asynchronous Digital Slope ADC.

A. Delay cell

Delay cells is shown in fig 2 which is used to know the amount of delay from input to output in a circuit and limits the overall conversion speed. when appling a power of 1 to pmos transistor (latch) is OFF, the DN is also 'OFF', and the reset is taking zero value the nmos transtor is 'OFF' in that situation the output of QN is "1" and QP is "0".

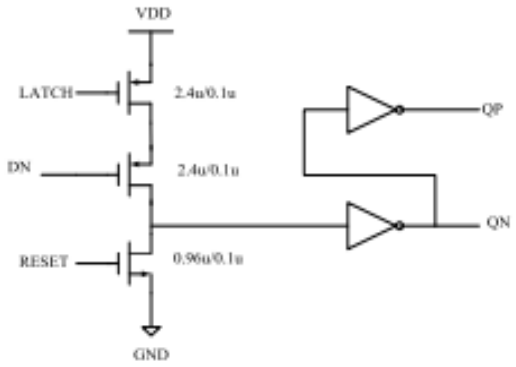

Fig 2: Delay Cell

B. Continous time comparator

Continous time comparator is shown in fig 3 in this the cross coupled inverters are connected to the latch, the signals are CLKP and CLKN are inputs those are called as sampling clock and inverted sampling clock. in this CLKN and EN are high, CLKP and EP are low then the comparator disabled. after sampling period CLKN turn into low and CLKP turn into high. in that time the continous time comparator is permitted to analyze the input signals. after completion of observation the output changes are EP enables from 0 to1 and EN enables from 1 to 0 then the output lines are given back to the comparator so that comparator instantly disables.

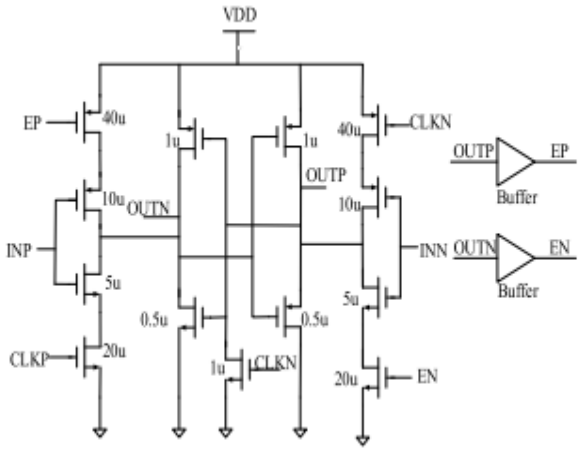

Fig 3: Continuous time comparator

C. Modified strong arm comparator

There are certain features of strong arm comparators, such as null static energy and rail to rail output directly. It takes a quick decision due to the positive feedback from the input differential stage, which can be achieved by two cross- connected pairs.

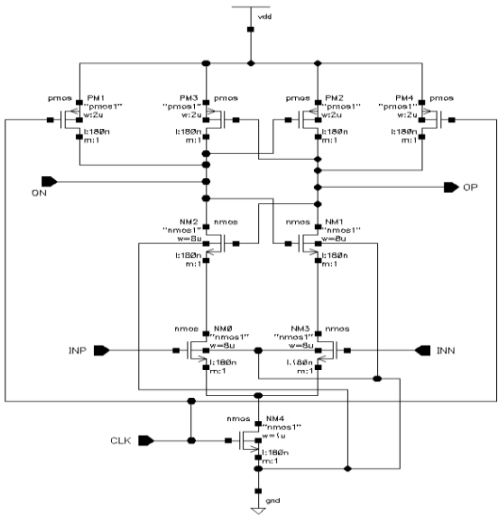

Fig 4: Modified strong arm comparator

We modified a strong arm Comparator for high speed without relying on complex calibration Schemes. The modified strong arm comparator is as shown in fig 4 it is used to speed up the sampling speed and also to reduce the propagation delay.

D. Pseudo NMOS SR-Latch

The NOR with a p-device is continually grounded or loaded with its door. An n-device pull down or a driver controls the input signal. NMOS technology is the sizeable equivalent of using an excess charge. It is called the 'pseudo NMOS.' The circuit can be used in a range o logical CMOS circuits. PMOS will be a linear region in this case for most of the time. Therefore, the resistance is small and therefore the time of RC is small. When a conductor reverses the present flows in the circuit on a continuous DC current. In SR-Latch two input NOR gate is replaced by a pseudo NMOS NOR Gate as shown in fig 5. The pseudo NMOS have a few transistors so the propagation delay can be lowered and improve the sampling speed.

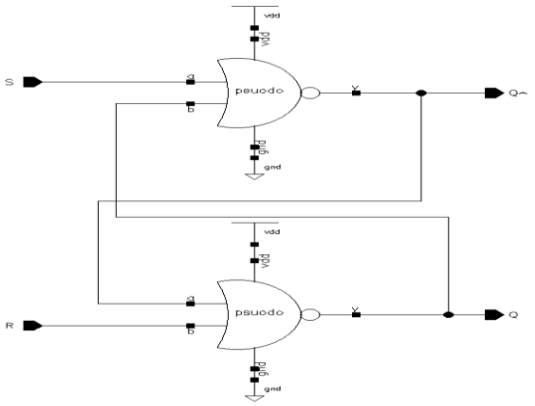

Fig 5: Pseudo NMOS SR-Latch

E. Decoder

The multiplexer based decoder is shown in Fig. 6 has lowest power dissipation. It requires a shorter critical path than the other kinds of decoders and has less hardware. Then this Structure is introduced to reduce power consumption. The multiplexers consist of a select signal generation referred as S. the output follows on the input when the S signal is at high level

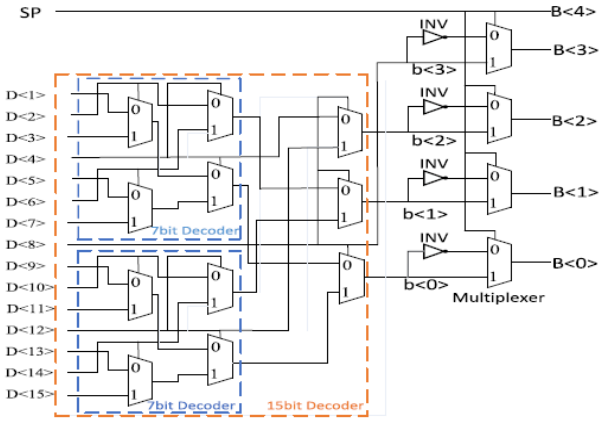

Fig 6: Multiplexer Based Decoder

When compare the other decoders the multiplexer based decoder can reduce the maximum delay

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III. SIMULATION RESULTS

In this selection signal generation block is modified by reducing the number of transistors that existed in asynchronous digital slope ADC. So, by reducing number of transistors that leads to increasing speed and reduces delay..

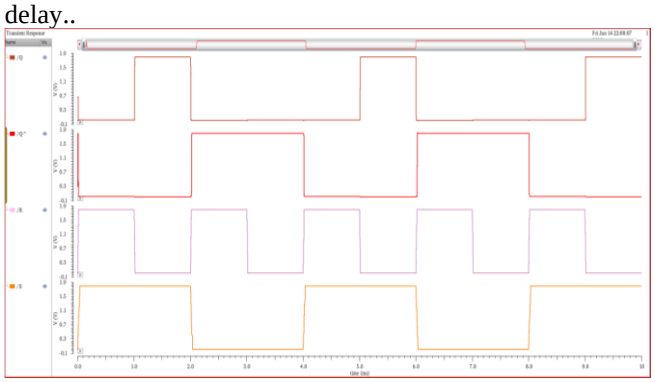

Fig 7: Pseudo NMOS SR-Latch Simulation Result

Fig 7 shows the transient response of Pseudo NMOS SR-Latch which is simulated by using gpdk 180nm technology in cadence virtuoso with power supply of 1.8V.

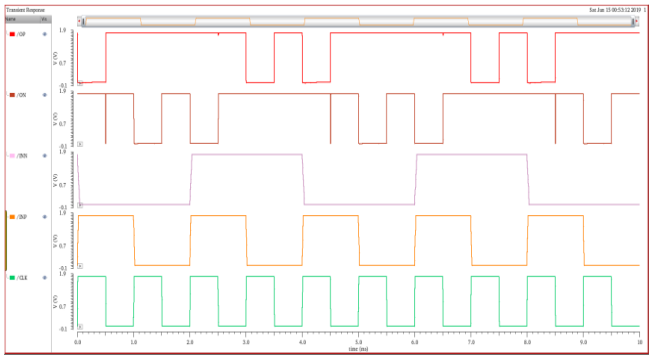

Fig 8: Modified Strong Arm Comparator Simulation Result

Fig 8 shows the transient response of Modified Strong Arm Comparator Result which is simulated by using gpdk 180nm technology in cadence virtuoso with power supply of 1.8V.

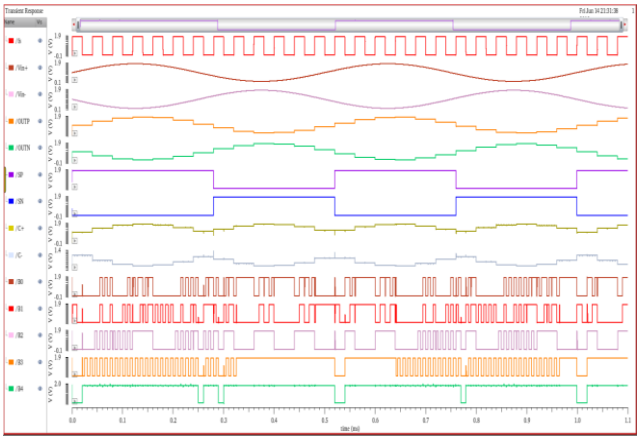

Fig 9: Asynchronous Digital Slope ADC Simulation Result

Fig 9 shows the transient response of ADS ADC Output Result which is simulated by using gpdk 180nm technology in cadence virtuoso with power supply of 1.8V.

The power and delay plot of asynchronous digital slope ADC. The delay is 133.67ns for the modified architecture and 0.0079uWpower.

Table1: delay and power

	DELAY	POWER
Asynchronous Digital Slope ADC	134.82nS	0.0083uW
Modified Asynchronous Digital Slope ADC	133.67nS	0.0079uW

IV. CONCLUSION

This paper introduces "A 5 bit 600MS/s asynchronous digital slope analog to digital converter to enhance the sampling rate with pseudo NMOS logic in SR Latch. In order to decrease the transistors, a modified strong arm comparator is suggested and continuous time is used in order to decrease dissipation of energy. Delay and power of asynchronous digital slope analog-to-digital converter is reduced by using a modified strong-arm comparator and continuous time comparator by comparing to existing asynchronous digital slope analog to digital converter.

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