International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-9 Issue-2, December, 2019

Power Factor Control in Multilevel Inverter with Dc Link Switches

M.Vijayalakshmi , V.Rengarajan , S.Mohanram , P.K.Mani

Abstract-The technology introduces a DC linked multi-level inverter topology to raise level of the efficiency and power factor. It consists of four active and four DC link switches for a proposed 5 level inverter .The number of level can be increased to 9, 13 and more levels as required. It uses a Phase Opposition Disposition method with a single carrier to control the switches.

Keywords- multilevel inverter, total harmonic distortion, DC links switches, single carrier.

I. INTRODUCTION

In recent times, inverters have found its manner into several fields of power grid analysis works, significantly within the space of the applications of power physics for power grid applications .To address the issues related to the 2 level electrical multi-level converters (MLIs) square measurement is introduced for grid connected inverter. The total harmonic distortion can be brought to low level using this proposed topology. Multilevel inverter technology can be splited into three categories – clamping neutral point, flying capacitor, and cascading type [1-2].MLIs can change their frequency and device voltage rating with the help of conventional 2 level electrical converters for an equivalent output voltage. Therefore, losses occurring in IGBT can be minimized which increases the efficiency of the system. [3-5]

II. MULTILEVEL INVERTER DESIGN

MLI comprises of 2 dc-link capacitors (C1, C2) and, and 4 active switches are placed between dc-link and H-bridge. 4 switching devices comprises a H-bridgeThe voltage across the dc-link is half of the dc output voltage and operated at a change frequency.Accordingly voltage across the H-bridge is total output dc voltage and the switches are switched at a frequency ofBasic output voltage ranging from 50 or 60 Hz.Thus, the dc -link switches and the adjacent H-bridge switches can be intentionally selected based on the power factor of the inverter system.In order to minimize the cost of the system and to raise the overall output efficiency

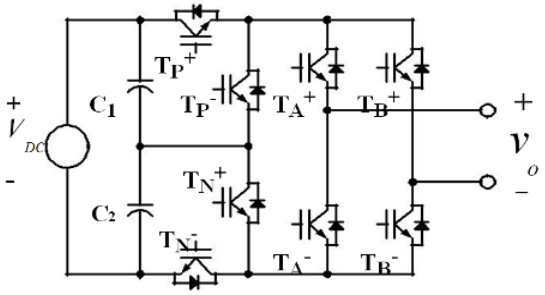

Fig. 1. DC linked multi-level inverter with single phase technology.

The 3 tendencies of the carrier signal square measure thought of to come up with the digital signal which is in pulse width modulation technique with the given signal, Phase disposition; which measures carriers square
measure in part.Alternative part opposition
disposition; where every carrier is part shifted by a nearing angle < 100from its adjacent carrier.Phaseopposition disposition; wherever the carriers on top of 0 voltage square measure a 100 and 80° out of part with those below 0 voltage.
A upcoming pulse signal strategy supporting opposition and disposition modulation which needs 1 carrier signal is planned and also the careful PWM is delineated in Fig. 4.If thereference signal is +ve, after that the pair of switches are off condition, and if it is -ve, then the pair of switches are in ON condition.Thus the switches composing the H bridge electrical converter is switched ON and OFF throughout the reference signal.Fig. 2.
Preparations of reference and carrier signal:
(a) PD.
(b) APOD.
(c) POD.
The voltage across the switch interference is total output voltage.

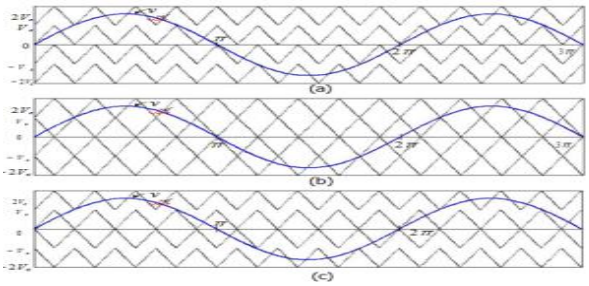

Fig. 2. Output signal for Carrier and reference waveforms for: (a) (PD). (b) (APOD). (c)(POD).

Revised Manuscript Received on December 30, 2019.
* Correspondence Author
M.Vijayalakshmi, Dept Of Eee, Vel Tech Multi Tech Dr.Rangarajan Dr.Sakunthala Engineering College, Chennai, India. Email: Mvijayalakshmi22@Gmail.Com
V.Rengarajan*, Dept Of Eee, Velammal Engineering College, Chennai, India. Email: Rengarajanv.Eee@Gmail.Com
S.Mohanram*, Dept Of Eee,Vel Tech Multi Tech Dr.Rangarajan Dr.Sakunthala Engineering College, Chennai, India. Email: Samsmr88@Gmail.Com
Dr.P.K.Mani*, Dept Of Eee,Vel Tech Multi Tech Dr.Rangarajan Dr.Sakunthala Engineering College, Chennai, India. Email: Manipudhurkannan@Gmail.Com

III. CIRCUIT OPERATION

The Operating Modes of Proposed system and output voltage are shows in table 1 has five levels) There are 4 operation modes depending on the rapid value of the reference voltage, and the maximum value of the carrier signal. Table II shows the possible inverter output values depending on the operating mode[6-8]The explanation for generating the signal with pulse width modulation for switches with dc links are given below.
1) Mode 1: If $V_{re\ f}$–V_c greater than carrier, then all switches T P+ and negative are turned on.
If vref –Vc less than carrier, then the switch TP+ or negative is turned off .
2) Mode 2:.If V_{ref} greater than carrier, then the switch positive or negative is turned on interchangeably. If V_{ref} less than carrier, then all switches positive and negative are turned off.
3) Mode 3:. If -V_{ref} greater than carrier, then the switch positive or negative is turned on interchangeably. If negative reference voltage isless than carrier, then all switches positive and negative are turned off.

TABLE 1 Output Voltage Levels

Operating mode	Reference voltage range	Output voltage
Mode 1	$V_c \le v_{ref} < 2V_c$	$V_{DC}/2$ or V_{DC}
Mode 2	$0 \le v_{ref} < V_c$	0 or V_{DC}
Mode 3	$-V_c \le v_{ref} < 0$	$-V_{DC}/2$ or 0
Mode 4	$-2V_c \le v_{ref} < -V_c$	$-V_{DC}$ or $-V_{DC}/2$

4) Mode 4: If -vref–Vc greater than v carrier, then all the switches of positive and negative are turned on.
If –Vrefand -Vc less than carrier, then the switches with positive and negative are turned off alternately.
Only1 carrier signal comeout with 8 PWM signals within the proposed method PWM methodology.
One of the problem that is to be addressed regarding multilevel electrical converter is used for the voltage balance of the dc link capacitance.
The voltage of first capacitance and second capacitance are to be maintained stable with half of the output dc voltage. However the voltage at the center is varied with the first and the second capacitance which is charged and discharged continuously.
If the voltage of the capacitance is unbalanced then the harmonic content will be higher which is present within the load current.

Table- II: Varying conditions of positive and negative switches

Output voltage (Vo)	Switching condition					
	T_P^+	T_P^-	T_N^+	T_N^-	T_A^+, T_B^-	T_A^-, T_B^+
V_{DC}	ON	OFF	OFF	ON	ON	OFF
$V_{DC}/2$	OFF	ON	OFF	ON	ON	OFF
	ON	OFF	ON	OFF	ON	OFF
0	OFF	ON	ON	OFF	ON	OFF
	OFF	ON	ON	OFF	OFF	ON
$-V_{DC}/2$	OFF	ON	OFF	ON	OFF	ON
	ON	OFF	ON	OFF	OFF	ON
$-V_{DC}$	ON	OFF	OFF	ON	OFF	ON

To find a solution to this method of executing the switching state it should be selected appropriately.
Likewise one switch with the DC link is turned on, the output voltage becomes fifty percent of the total dc output voltage.

IV. EXPANSION FOR DEVELOPED VERSION OF INVERTER

The total number of devices with the switch in the developed fifth level inverter(fig.1) is resembling the conventional h-bridge converter in cascaded method.

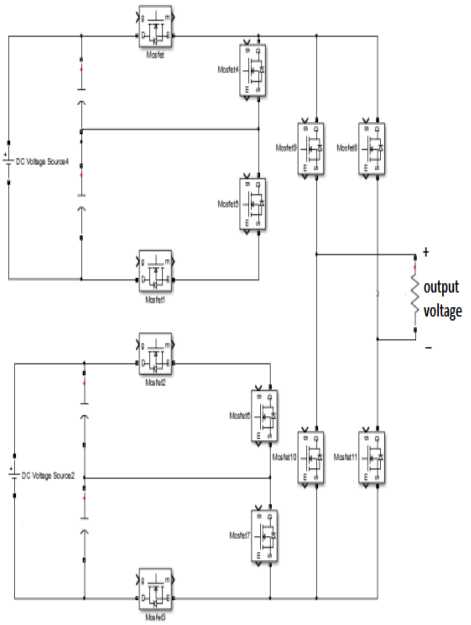

FIG. 3 Circuit For 9 Level Inverter

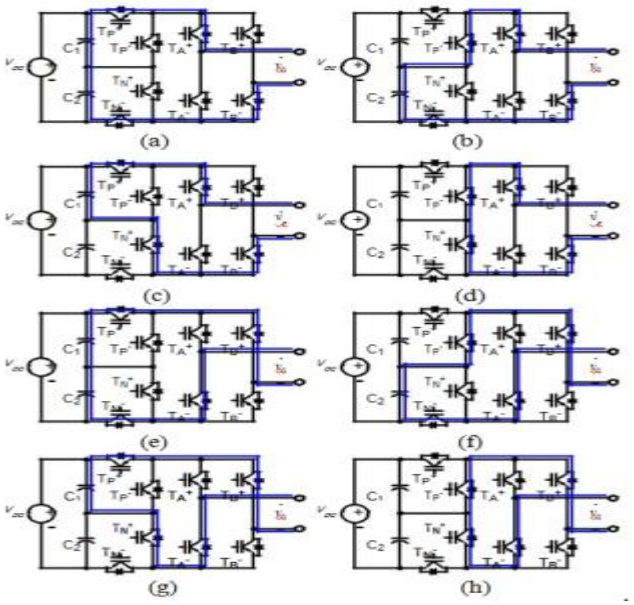

Fig. 4 Modes of operation

There is a condition of maximizing the efficiency of the given multilevel inverter, nineth level inverter is also proposed the overall circuit diagram is explained in (fig.3).

It is given in the figure in which the proposed system which has the requirement of minimum devices which has the cascaded h bridge nine level multilevel inverter. Consequently, the total number of switches in the designed multilevel inverter is minimized.

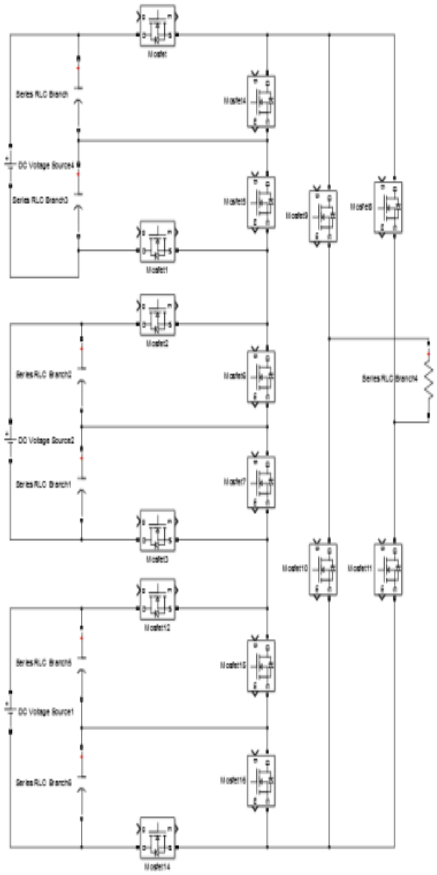

Fig .5 Inverter with 13 level switches

V. RESULTS OF THE SIMULATION

The projected 5-level electrical converter is tested for verification by introducing LC as the load.

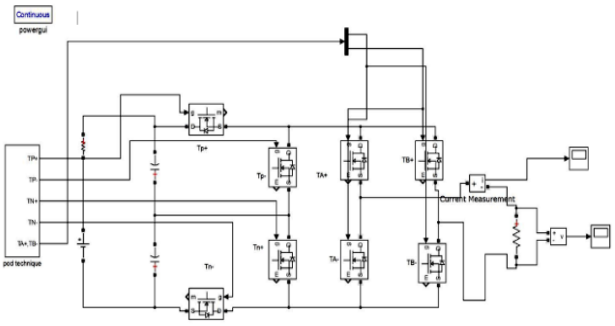

Fig. 6 simulation circuit of dc linked multi level inverter with single phase technology

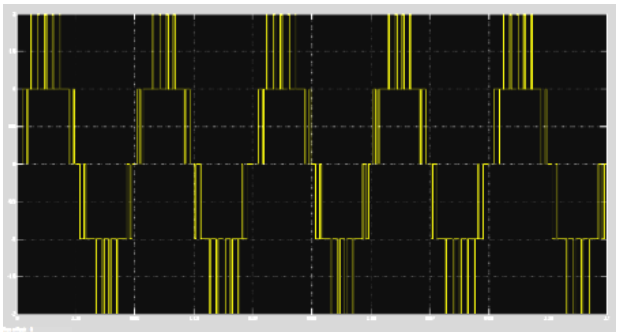

Fig.7. simulated voltage waveform

Fig. 7 and 8 show output voltage - load voltage & current

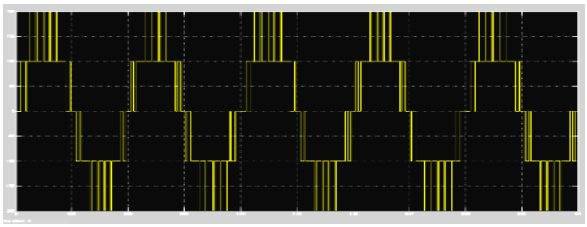

Fig.8 simulated current waveform.

The output results have the base with the experiment which is conducted with various rated parameters.
The entire technology were found equal to that of the simulation result.

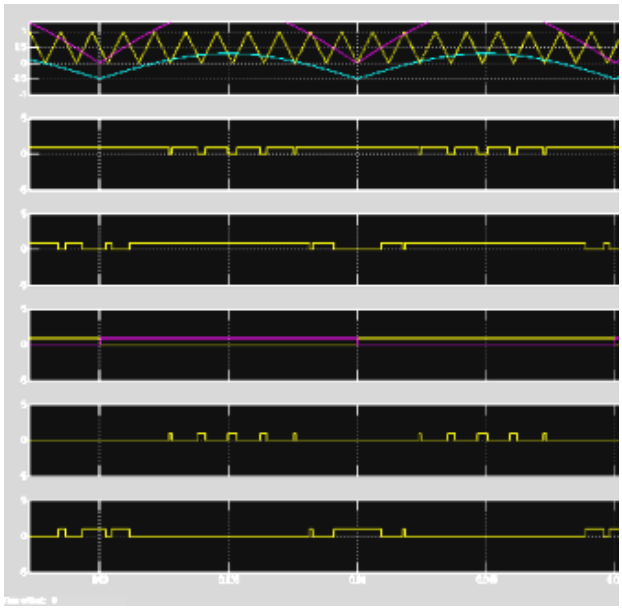

Fig 9. Waveform Of The Switching Devices
The Voltage Of The Capacitor Are Being Balanced At The Voltage Of 100v.

VI.CONCLUSION

The paper has the detailed explanation about a unused technique for multilevel electrical converter technology supported by inverter bridge technology in H level electrical converter has switches in four numbers which is inter linked with dc source. The givens system has the advantages listed below as the Number of devices used are reduced which is that of the traditional multilevel inverters.

So far, the projected design is a lot of reliability with efficient performance and value competitive than the traditional multilevel and construction inverters. The fourth level switches are operated at minimum frequency with 60 hertz. Consequently, the losses of the four switches are almost negligible. Only 1 carrier signal for PWM signals for four change devices. The developed technology can be extended to 9or maximum level with decreased active equipment count to the part of the inverter.

REFERENCES

1. "A power-line conditioner supported flying- electrical device construction voltage supply device with phase-shift SPWM" Y. Liang, C.O.Nwankpa, IEEE Trans. Industrial Electronics, Vol. 36, pp. 965-971, 2000.
2. "Control of a Single- Phase Cascaded H- Bridge construction electrical converter for Grid- Connected electrical phenomenon Systems", E. Villanueva, P. Correa, M.Pacas, IEEE Trans. Industrial Electronics, Vol.56,pp.4399-4406,2009.
3. "Multilevel transformer less topologies for single-phase grid-connected converters" O. Lopez, R. Teodorescu, J.Doval-Gandoy, IEEE.IECON 2006, pp. 5191-5196, 2006.
4. "The analysis of conduction and switching losses in multi-level inverter system", Tae-Jin Kim, Dae-Wook Kang, Yo-Han Lee and Dong-Seok Hyun, PESC. 2001 IEEE Vol. 3, pp1363-1368,2001.
5. "Comparison of Neutral-Point- Clamped, Symmetrical, and Hybrid Asymmetrical Multilevel Inverters", D.A.B. Zambra, C. Rech, J.R. Pinheiro, IEEE Trans.Ind. Electron., Vol.57,no.7,pp2297-2306,July2010.
6. "Analysis of SFCL's in DC System with Renewable Energy Sources" S.Mohanram, R.Chandralekha ,in International Journal of Engineering and Technology 7(6):2084-2091 • January 2016

AUTHORS PROFILE

Mrs.M.Vijayalakshmi has completed her B.E. Electrical and Electronics Engineering and M.E. Power Electronics and Drives at Anna University, Chennai. At present she is working as Assistant Professor in Electrical and Electronics Engineering Dept, Vel Tech MultitTech Dr.Rangarajan Dr.SakunthalaEngineering College, Chennai-600062. Her fields of interest are, Renewable Energy Systems and Battery Management.
Email: mvijayalakshmi22@gmail.com

Mr.V.Renagarajan has completed his B.E. Electrical and Electronics Engineering and M.E. Power Electronics and Drives at Anna University, Chennai. At present he is working as Assistant Professor in Electrical and Electronics Engineering Dept, velammal engineering College, Chennai-600066. He is a Life Member of ISTE and Member of IE(I). His fields of interest are, power quality Energy Systems, optimum power management, electric vehicles and Battery Management.
Email:rengarajanv.eee@gmail.com

Mr.Mohanram has completed his B.E. Electrical and Electronics Engineering and M.E Embedded System Technology at Anna University, Chennai. At present he is working as Assistant Professor in Electrical and Electronics Engineering Dept, Vel Tech MultitTech Dr.Rangarajan Dr.Sakunthala Engineering College, Chennai-600062.Her fields of interest are, embedded networking advanced embedded systems Systems and He has published 13 research papers from his research works in reputed International journals
Email: samsmr88@gmail.com

Dr.P.K.Mani has completed his B.E. Electrical and Electronics Engineering and M.E. Power Systems Engineering at Anna University, Chennai .He has completed his Ph.D. in Electrical and Electronics Engineering at Vel Tech Rangarajan Dr.Sagunthal R&D Institute of Science and Technology. At present he is working as Associate Professor in Electrical and Electronics Engineering Dept, Vel Tech Multi Tech Dr.Rangarajan Dr.Sakunthala Engineering College, Chennai-600062. He has published 14 research papers from his research works in reputed International journals. He is a Life Member of ISTE and Member of IENAG. He has 19 years of teaching experience and 10 years of industrial experience. His fields of interest are Intelligent Techniques used for Power Quality Improvement, Renewable Energy Systems and Battery Management.